23. General PWM Timer (GPT)

23.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

This GPT provides the high resolution PWM waveform generation function for the channel 0 to 3, the A/D conversion start request function, the asymmetric automatic dead time setting function, and the enhanced interrupt skipping function. In addition, it is enhanced with the external pulse width measuring function for the channel 0 to 3, the additional PWM modes for the channel 4 to 9, the extended buffer transfer function, the GTCPPO pin output function, and the inter-channel cooperation function.

Table 23.1 lists the GPT specifications, Table 23.2 shows the GPT functions, and Figure 23.1 shows a block diagram.

Table 23.1 GPT specifications

Item	Description
Functions	● 32 bits × 14 channels (GPT32n (n = 0 to 13)) ● Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter ● Clock sources independently selectable for each channel ● Two input/output pins per channel ● Two output compare/input capture registers per channel ● For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use ● In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms ● Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow ● Generation of dead times in PWM operation ● Generation of high accuracy duty in the vicinity of duty 0% and 100% PWM waveform ● In output compare operation, setting compare register is immediately used to generate PWM waveform with dead times ● Synchronous starting, stopping and clearing counters for arbitrary channels ● Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 8 ELC events ● Count start, count stop, count clear, up-count, down-count, or input capture operation in response to the status of two input pins ● Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 4 external triggers ● Output pin disable function by dead time error and detected short-circuits between output pins ● A/D conversion start request generation function ● PWM waveform for controlling brushless DC motors can be generated ● Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC ● Enables the noise filter for input capture and input UVW ● Period count function ● External pulse width measuring function ● Logical operation between the channel output ● Synchronous counter clearing/counter setting/input capture among channels ● Bus clock: PCLKA, Core clock: GTCLK[*1] ● Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64) (when using synchronous clock), PCLKA ≤ GTCLK (when using asynchronous clock GTIOCnA/B input/output pin polarity reversal function)

Note 1. GPT core clock (GTCLK) is PCLKD when synchronous clock is selected, and GPTCLK when asynchronous clock is selected. See Figure 23.3.

Table 23.2 GPT functions (1 of 2)

Parameter		Description
Count clock		GTCLK GTCLK/2 GTCLK/4 GTCLK/8 GTCLK/16 GTCLK/32 GTCLK/64 GTCLK/128 GTCLK/256 GTCLK/512 GTCLK/1024 GTETRGA, GTETRGB, GTETRGC, GTETRGD
Output compare/input capture registers (GTCCR)		GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register		GTPR
Cycle setting buffer register		GTPBR GTPDBR
I/O pins		GTIOCnA GTIOCnB (n = 0 to 13)
External trigger input pin*1		GTETRGA GTETRGB GTETRGC GTETRGD
Counter clear sources		GTPR register compare match Input capture Input pin status ELC event input GTETRGn (n = A to D) pin input GTCCR register compare match (GPT32n (n = 4 to 9)) Other channel's counter clear sources (GPT32n (n = 4 to 9))
Period count function		Available (GPT32n (n = 0 to 3, 10 to 13))
Compare match output	Low output	Available
	High output	Available
	Toggle output	Available
Input capture function		Available
Automatic addition of dead time		Available
PWM mode		Available
High accuracy PWM waveform		Available (GPT32n (n = DEADBEEF))
Phase count function		Available
External pulse width measuring function		Available
Buffer operation		Double buffer Simultaneous operation disable control for multiple channels Buffer operation by counter clearing/compare match
One-shot operation		Available
DMAC/DTC activation		All the interrupt sources
A/D conversion start request		Compare match of GTADTRA or GTADTRB register
Brushless DC motor control function		Available

Table 23.2 GPT functions (2 of 2)

Parameter	Description
Interrupt sources	11 sources ● GTCCRA compare match/input capture(GPTn_CCMPA) ● GTCCRB compare match/input capture(GPTn_CCMPB) ● GTCCRC compare match(GPTn_CMPC) ● GTCCRD compare match(GPTn_CMPD) ● GTCCRE compare match(GPTn_CMPE) ● GTCCRF compare match(GPTn_CMPF) ● GTCNT overflow (GTPR compare match) (GPTn_OVF) ● GTCNT underflow (GPTn_UDF) ● GTPC count stop(GPTx_PC) (x = 0 to 3)
Interrupt skipping function	● Skipping of interrupts of GTCNT counter overflow (GTPR register compare match) (GTPn_OVF) and GTCNT counter underflow (GTPn_UDF) (interlocked with other interrupts and A/D conversion start requests) ● Skipping of GTADTRA and GTADTRB register compare match (GPT32y (y = 4 to 9)) ● Buffer operation skipping function
Event linking (ELC) function	Available*2
Noise filtering function	Available
Logical operation between the channel output	Available
Synchronous counter clearing/counter setting/input capture	Available (GPT32n (n = 4 to 9))
TrustZone Filter	Security and Privilege attribution can be set for each UNIT.*3

Note:
Note 1. GTETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPCRD.MSTPDn (n = 11 to 14) bit.
Note 2. See section 23.6. Operations Linked by ELC.
Note 3. UNIT0 to UNIT3 is CH0 to CH3.
UNIT4 is CH4 to CH9.
UNIT5 to 8 is CH10 to CH13.

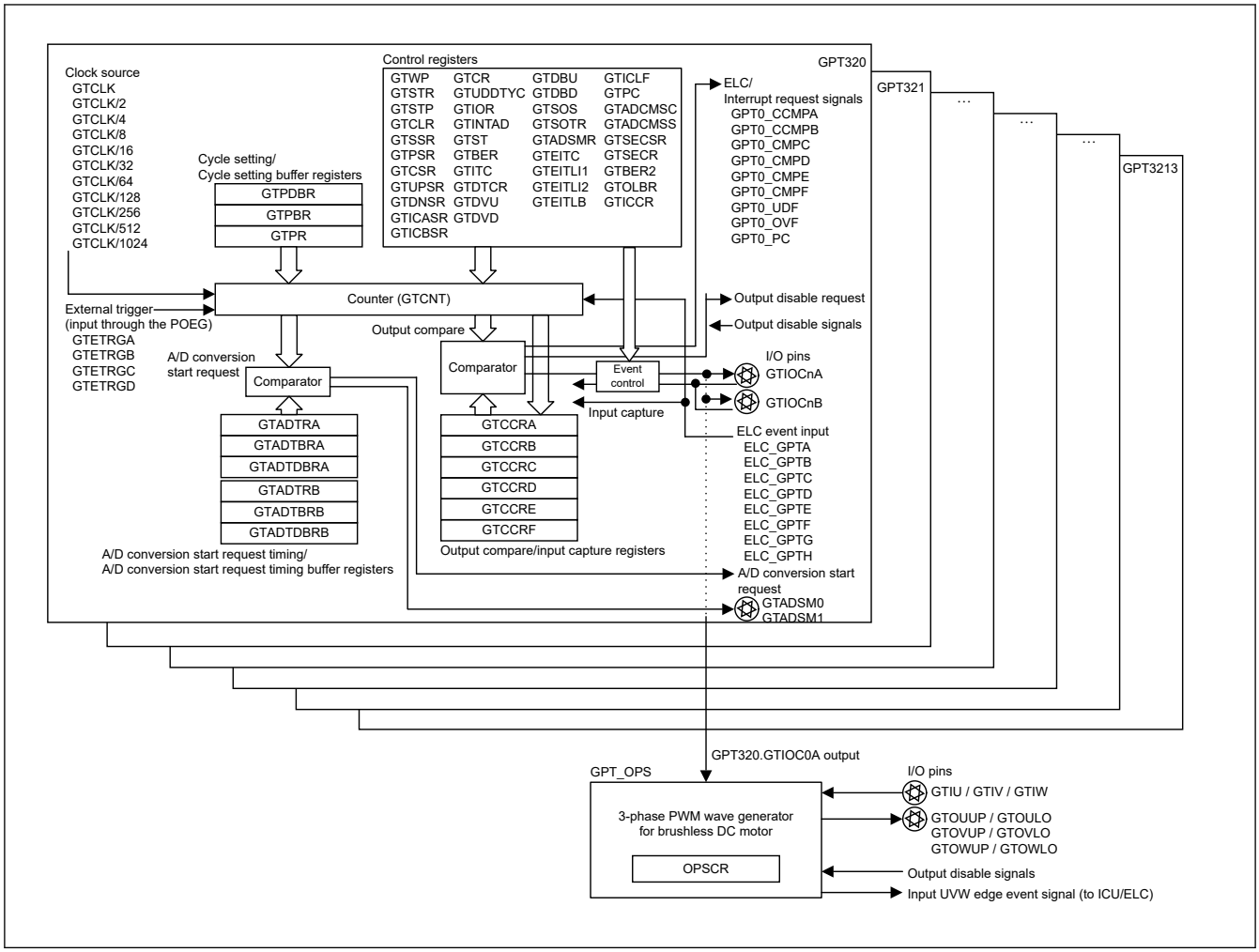


Figure 23.1 GPT block diagram (Saw-wave PWM mode 1, Saw-wave one-shot pulse mode, Triangle-wave PWM mode1,2,3)

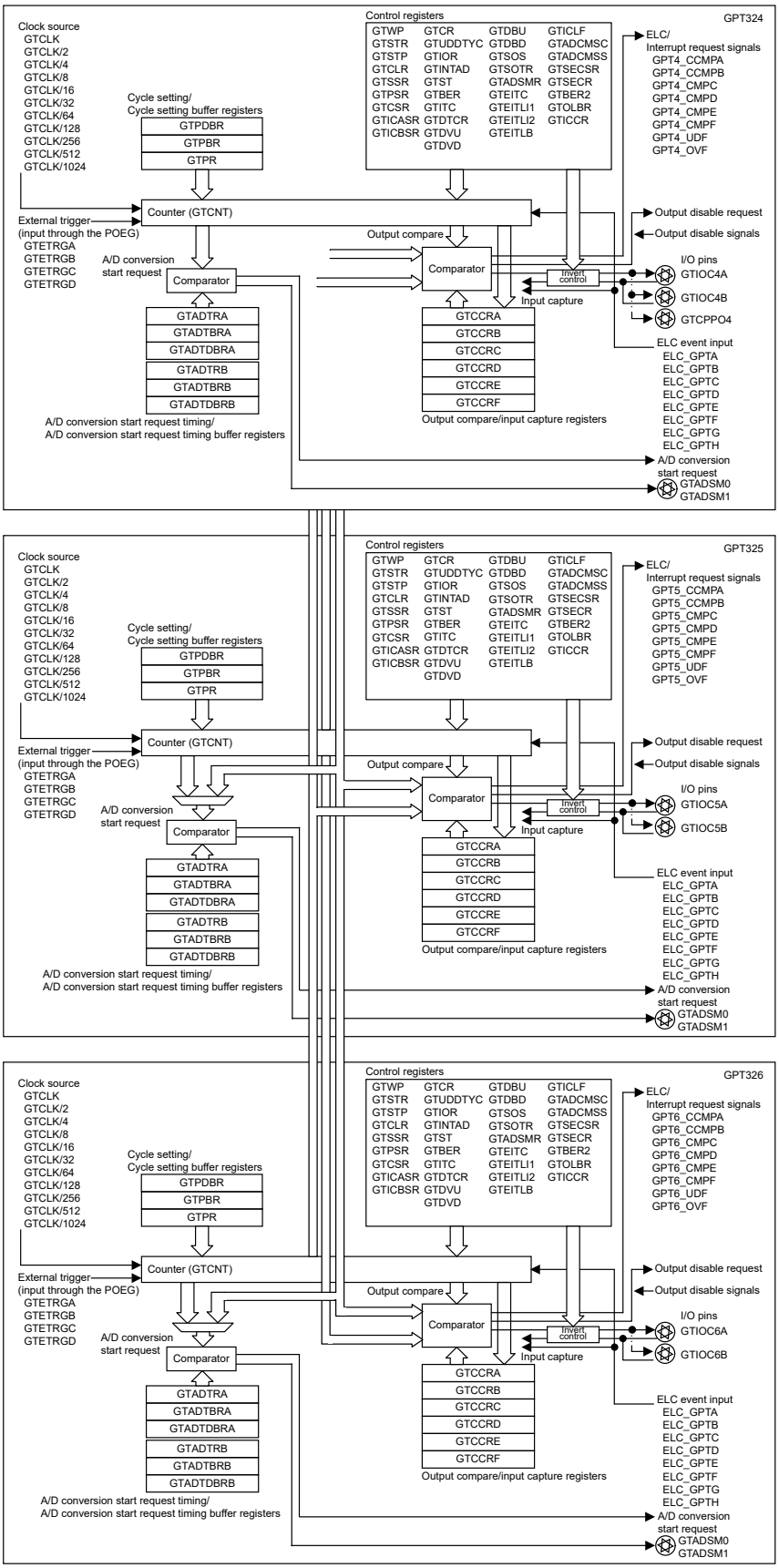


Figure 23.2 GPT block diagram (Saw-wave PWM mode 1, 2, Saw-wave one-shot pulse mode, Triangle-wave PWM mode1,2,3, Complementary PWM mode 1, 2, 3, 4)

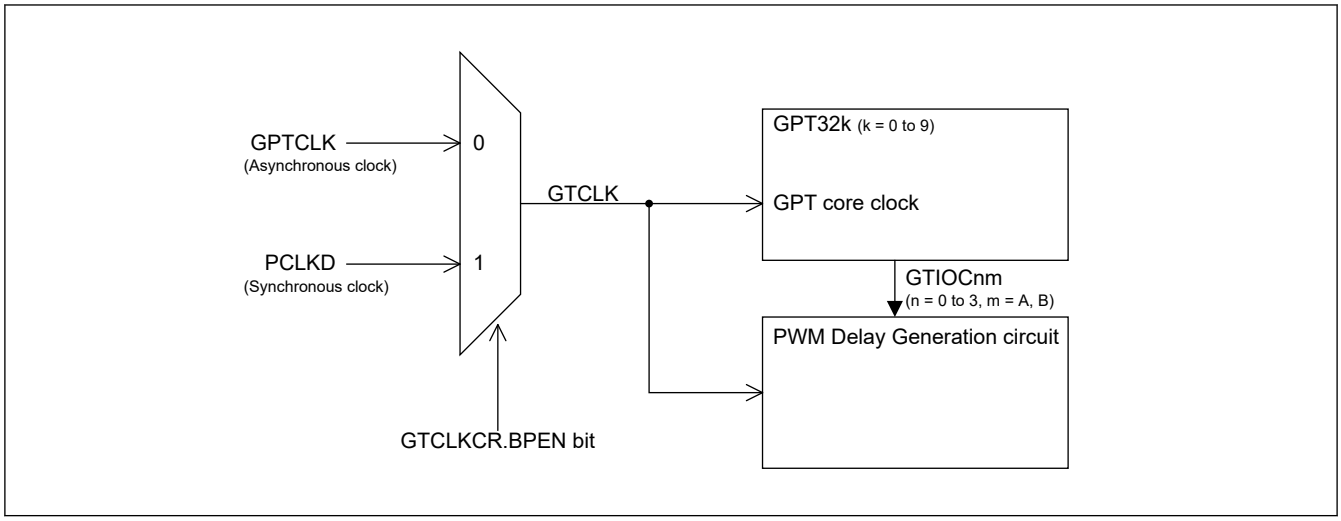


Figure 23.3 GPT core clock selection diagram

In this specification, three consecutive channels to configure complementary PWM mode is defined as complementary PWM mode channel group. The lowest position channel of complementary PWM mode channel group is defined as master channel. The second channel is defined as slave channel 1. The highest position channel is defined as slave channel 2.

Figure 23.4 shows an example using multiple GPTs.

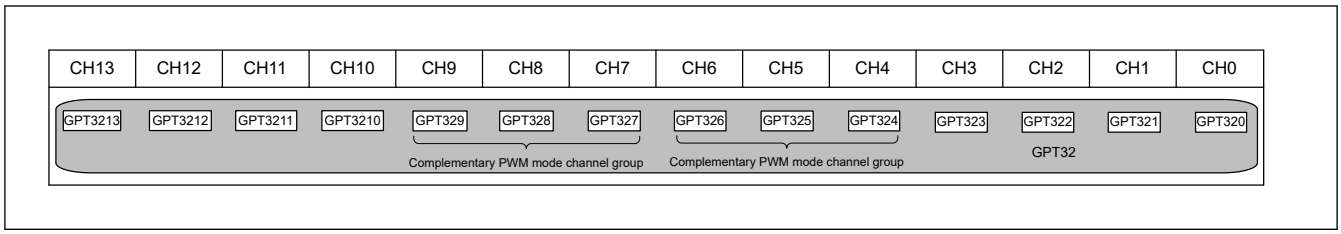


Figure 23.4 Association between GPT channels and module names

Table 23.3 lists the I/O pins.

Table 23.3 GPT I/O pins

Channel	Pin name	I/O	Function
Common	GTETRGx	Input	External trigger input pin x (input through the POEG)
	GTADSM0	Output	A/D conversion start request monitor 0 output pin
	GTADSM1	Output	A/D conversion start request monitor 1 output pin
GPT32n	GTIOCnA	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOCnB	I/O	GTCCRB register input capture input/output compare output/PWM output pin
	GTCPPOk	Output	Toggle output synchronized with PWM period
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

Note: x: A to D
n: 0 to 13
k: 0 to 13

23.2 Register Descriptions

23.2.1 GTWP : General PWM Timer Write-Protection Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	CMNWP	CLRWP	STPWP	STRWP	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	Register Write Disable 0: Write to the register enabled 1: Write to the register disabled	R/W
1	STRWP	GTSTR.CSTRT Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
2	STPWP	GTSTP.CSTOP Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
3	CLRWP	GTCLR.CCLR Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
4	CMNWP	Common Register Write Disabled 0: Write to the register is enabled 1: Write to the register is disabled	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
15:8	PRKEY[7:0]	GTWP Key Code When 0xA5 is written to these bits, writing to the WP, STRWP, STPWP, CLRWP, and CMNWP bits are permitted. These bits are read as 0.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

GTWP enables or disables writing to registers to prevent accidental modification. Protection by the GTWP register is only for the writes by the CPU. GTWP does not protect registers from updates that occur in association with CPU writes.

WP bit (Register Write Disable)

The following is a list of write enabled or disabled registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTEITC, GTEITLI1, GTEITLI2, GTEITLB, GTICLF, GTPC, GTADCMSC, GTADCMSS, GTBER2, GTOLBR, GTICCR.

STRWP bit (GTSTR.CSTRT Bit Write Disable)

The STRWP bit enables or disables starting the updating of counter values by writing to the CSTRTn bit (n = 0 to 13) corresponding to a channel number in the GTSTR register.

The bit position of each CSTRTn bit in the GTSTR register is allocated to the channel with the corresponding number, and writing to the GTSTR register for any channel results in writing to the registers of all channels. The STRWP bit for

each channel does not control writing but only controls updating of the CSTRT bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CSTRT bits of a channel for which the setting of the STRWP bit is 1 (disabling writing), the CSTRT bit for the given channel is not updated, but the CSTRT bits corresponding to channel for which the setting of the STRWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT320.GTWP.STRWP bit is 0 (enabling writing), writing 1 to the GPT321.GTSTR.CSTRT0 bit when its current setting is 0 causes the value to be updated, and the GPT320.GTCNT counter starts to run. When the setting of the GPT320.GTWP.STRWP bit is 1 (disabling writing), writing 1 to the GPT321.GTSTR.CSTRT0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT320.GTCNT counter does not run.

If you want to protect all bits in the GTSTR register from being updated, set the STRWP bits of all channels to 1.

STPWP bit (GTSTP.CSTOP Bit Write Disable)

The STPWP bit enables or disables starting the updating of counter values by writing to the CSTOPn bit (n = 0 to 13) corresponding to a channel number in the GTSTP register.

The bit position of each CSTOPn bit in the GTSTP registers is allocated to the channel with the corresponding number, and the writing to the GTSTP register for any channel results in writing to the registers of all channels. The STPWP bit for each channel does not control writing but only controls updating of the CSTOP bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CSTOP bits of a channel for which the setting of the STPWP bit is 1 (disabling writing), the CSTOP bit for the given channel is not updated, but the CSTOP bits corresponding to channel for which the setting of the STPWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT320.GTWP.STPWP bit is 0 (enabling writing), writing 1 to the GPT321.GTSTP.CSTOP0 bit when its current setting is 0 causes the value to be updated, and the GPT320.GTCNT counter is stopped. When the setting of the GPT320.GTWP.STPWP bit is 1 (disabling writing), writing 1 to the GPT321.GTSTP.CSTOP0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT320.GTCNT counter is not stopped.

If you want to protect all bits in the GTSTP register from being updated, set the STPWP bits of all channels to 1.

CLRWP bit (GTCLR.CCLR Bit Write Disable)

CLRWP bit enables or disables starting the updating of counter values by writing to the CCLRn bit (n = 0 to 13) corresponding to a channel number in the GTCLR register.

The bit position of each CCLRn bit in the GTCLR registers is allocated to the channel with the corresponding number, and the writing to the GTCLR register for any channel results in writing to the registers of all channels. The CLRWP bit for each channel does not control writing but only controls updating of the CCLR bit for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the CCLR bits of a channel for which the setting of the CLRWP bit is 1 (disabling writing), the CCLR bit for the given channel is not updated, but the CCLR bits corresponding to channel for which the setting of the CLRWP bit is 0 (enabling writing) are updated. For example, when the setting of the GPT320.GTWP.CLRWP bit is 0 (enabling writing), writing 1 to the GPT321.GTCLR.CCLR0 bit when its current setting is 0 causes the value to be updated, and the GPT320.GTCNT counter is cleared. When the setting of the GPT320.GTWP.CLRWP bit is 1 (disabling writing), writing 1 to the GPT321.GTCLR.CCLR0 bit when its current setting is 0 leaves the bit with the value 0, and the GPT320.GTCNT counter is not cleared.

If you want to protect all bits in the GTCLR register from being updated, set the CLRWP bits of all channels to 1.

CMNWP bit (Common Register Write Disabled)

CMNWP bit enables or disables starting the updating of counter values by writing to the SECSELn bit (n = 0 to 13) corresponding to a channel number in the GTSECSR register or to the GTSECR register.

The bit position of each SECSEL bit in the GTSECSR registers is allocated to the channel with the corresponding number, and the writing to the GTSECSR register for any channel results in writing to the registers of all channels. Writing to the GTSECR register of any channel leads to writing to the registers of all channels. The CMNWP bit for each channel does not control writing but only controls updating of the SECSEL bit and the GTSECR register value for the corresponding channel when simultaneously writing to all channels.

Therefore, when writing to the SECSEL bit and the GTSECR register value of a channel for which the setting of the CMNWP bit is 1 (disabling writing), the SECSEL bit and the GTSECR register value for the given channel is not updated,

but the SECSEL bit and the GTSECR register value corresponding to channel for which the setting of the CMNWP bit is 0 (enabling writing) are updated.

For example, when the setting of the GPT320.GTWP.CMNWP bit is 0 (enabling writing), writing to the GPT321.GTSECSR.SECSEL0 bit causes the value of the GPT320.GTSECSR.SECSEL0 bit to be updated. In the same way, writing to the GPT321.GTSECR register updates the value of the GPT320.GTSECR register. When the setting of the GPT320.GTWP.CMNWP bit is 1 (disabling writing), writing to the GPT321.GTSECSR.SECSEL0 bit does not cause the value of the GPT320.GTSECSR.SECSEL0 bit to be updated. In the same way, writing to the GPT321.GTSECR register does not update the value of the GPT320.GTSECR register.

If you want to protect all bits in the GTSECSR and GTSECR registers from being updated, set the CMNWP bits of all channels to 1.

PRKEY[7:0] bit (GTWP Key Code)

This bit controls whether the WP, STRWP, STPWP, CLRWP, and CMNWP bits can be overwritten.

23.2.2 GTSTR : General PWM Timer Software Start Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x04

Bit position:	31																															0
Bit field:	CSTRT31 to CSTRT0																															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	Channel n GTCNT Count Start (n is the same as the bit position value) 0: GTCNT counter is not started 1: GTCNT counter is started	R/W

Note 1. The bits that can be used vary depending on the product. The n in CSTRTn is the same as the GPT channel number. For this product, n is 0 to 13.

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0 to 13.

The GTSTR bit number represents the channel number. The GTSTR register of each channel is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTR register.

In complementary PWM mode, writing to the CSTRTn bit of master channel is only valid. The bit on slave channels reflects the bit value of master channel.

For the association between module names and channel numbers, see Figure 23.4.

CSTRTn bits (Channel n GTCNT Count Start (n = 0 to 13))

The CSTRTn bits start channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0 to 13) has no effect unless the GTSSR.CSTRT bit is set to 1.

The read data shows the counter status of each channel (GTCR.CST bit). A value of 0 means the counter is stopped and 1 means the counter is running.

23.2.3 GTSTP : General PWM Timer Software Stop Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x08

Bit position:	31																														0
Bit field:	CSTOP31 to CSTOP0																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	Channel n GTCNT Count Stop (n is the same as the bit position value) 0: GTCNT counter is not stopped 1: GTCNT counter stopped	R/W

Note 1. The bits that can be used vary depending on the product. The n in CSTOPn is the same as the GPT channel number. For this product, n is 0 to 13.

The GTSTP stops the GTCNT counter operation for each channel n, where n = 0 to 13.

The GTSTP bit number represents the channel number. The GTSTP register of each channel is shared by all the channels. The GTCNT counter stops for the channel associated with the GTSTP bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTP register.

In complementary PWM mode, writing to the CSTOPn bit of master channel is only valid. The bit on slave channels reflects the bit value of master channel.

For the association between module names and channel numbers, see Figure 23.4.

CSTOPn bits (Channel n GTCNT Count Stop (n = 0 to 13))

The CSTOPn bits stop channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0 to 13) has no effect unless the GTPSR.CSTOP bit is set to 1. The read data shows the counter status of each channel (invert of GTCR.CST bit). A value of 0 means the counter is running and 1 means the counter is stopped.

23.2.4 GTCLR : General PWM Timer Software Clear Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x0C

Bit position:	31																														0
Bit field:	CCLR31 to CCLR0																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	Channel n GTCNT Count Clear (n : the same as bit position value) 0: GTCNT counter is not cleared 1: GTCNT counter is cleared	W

Note 1. The bits that can be used vary depending on the product. The n of CCLRn is the same as the GPT channel number. For this product, n is 0 to 13.

The GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0 to 13.

The GTCLR bit number represents the channel number. The GTCLR register of each channel is shared by all the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter.

In complementary PWM mode, writing to the CCLRn bit of master channel is only valid. The bit on slave channels reflects the bit value of master channel.

For the association between module names and channel numbers, see Figure 23.4.

CCLRn bits (Channel n GTCNT Count Clear (n = 0 to 13))

When the counting direction flag is set for decrement (GTST.TUCF flag = 0) with saw-wave mode selected in the GTCR.MD[2:0] bits, the value of the GTCNT counter becomes that of the corresponding GTPR register in response to writing 1 to the CCLRn bit. The value of the counter becomes 0x0000 0000 with other settings. These bits are read as 0.

23.2.5 GTSSR : General PWM Timer Start Source Select Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGA input 1: Counter start enabled on the rising edge of GTETRGA input	R/W*1
1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGA input 1: Counter start enabled on the falling edge of GTETRGA input	R/W*1
2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGB input 1: Counter start enabled on the rising edge of GTETRGB input	R/W*1
3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGB input 1: Counter start enabled on the falling edge of GTETRGB input	R/W*1
4	SSGTRGCR	GTETRGC Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGC input 1: Counter start enabled on the rising edge of GTETRGC input	R/W*1
5	SSGTRGCF	GTETRGC Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGC input 1: Counter start enabled on the falling edge of GTETRGC input	R/W*1
6	SSGTRGDR	GTETRGD Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGD input 1: Counter start enabled on the rising edge of GTETRGD input	R/W*1
7	SSGTRGDF	GTETRGD Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGD input 1: Counter start enabled on the falling edge of GTETRGD input	R/W*1
8	SSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	SSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W

Bit	Symbol	Function	R/W
10	SSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	SSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	SSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	SSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	SSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	SSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	SSELCA	ELC_GPTA Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTA input 1: Counter start enabled at the ELC_GPTA input	R/W*1
17	SSELCB	ELC_GPTB Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTB input 1: Counter start enabled at the ELC_GPTB input	R/W*1
18	SSELCC	ELC_GPTC Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTC input 1: Counter start enabled at the ELC_GPTC input	R/W*1
19	SSELCD	ELC_GPTD Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTD input 1: Counter start enabled at the ELC_GPTD input	R/W*1
20	SSELCE	ELC_GPTE Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTE input 1: Counter start enabled at the ELC_GPTE input	R/W*1
21	SSELCF	ELC_GPTF Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTF input 1: Counter start enabled at the ELC_GPTF input	R/W*1
22	SSELCG	ELC_GPTG Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTG input 1: Counter start enabled at the ELC_GPTG input	R/W*1
23	SSELCH	ELC_GPTH Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTH input 1: Counter start enabled at the ELC_GPTH input	R/W*1
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTRT	Software Source Counter Start Enable 0: Counter start disabled by the GTSTR register 1: Counter start enabled by the GTSTR register	R/W*1

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

The GTSSR sets the source to start the GTCNT counter.

Input from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGB pin input.

SSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Start Enable)

The SSGTRGCR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGC pin input.

SSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Start Enable)

The SSGTRGCF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGC pin input.

SSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Start Enable)

The SSGTRGDR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGD pin input.

SSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Start Enable)

The SSGTRGDF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGD pin input.

SSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

SSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

SSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

SSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

SSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

SSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

SSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

SSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to H)

The SSELCm bit enables or disables the GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables the GTCNT counter start by GTSTR register.

23.2.6 GTPSR : General PWM Timer Stop Source Select Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGA input 1: Counter stop enabled on the rising edge of GTETRGA input	R/W*1
1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGA input 1: Counter stop enabled on the falling edge of GTETRGA input	R/W*1
2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGB input 1: Counter stop enabled on the rising edge of GTETRGB input	R/W*1
3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGB input 1: Counter stop enabled on the falling edge of GTETRGB input	R/W*1
4	PSGTRGCR	GTETRGC Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGC input 1: Counter stop enabled on the rising edge of GTETRGC input	R/W*1
5	PSGTRGCF	GTETRGC Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGC input 1: Counter stop enabled on the falling edge of GTETRGC input	R/W*1

Bit	Symbol	Function	R/W
6	PSGTRGDR	GTETRGD Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGD input 1: Counter stop enabled on the rising edge of GTETRGD input	R/W*1
7	PSGTRGDF	GTETRGD Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGD input 1: Counter stop enabled on the falling edge of GTETRGD input	R/W*1
8	PSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	PSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	PSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	PSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	PSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	PSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	PSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	PSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	PSELCA	ELC_GPTA Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTA input 1: Counter stop enabled at the ELC_GPTA input	R/W*1
17	PSELCB	ELC_GPTB Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTB input 1: Counter stop enabled at the ELC_GPTB input	R/W*1
18	PSELCC	ELC_GPTC Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTC input 1: Counter stop enabled at the ELC_GPTC input	R/W*1
19	PSELCD	ELC_GPTD Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTD input 1: Counter stop enabled at the ELC_GPTD input	R/W*1

Bit	Symbol	Function	R/W
20	PSELCE	ELC_GPTE Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTE input 1: Counter stop enabled at the ELC_GPTE input	R/W*1
21	PSELCF	ELC_GPTF Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTF input 1: Counter stop enabled at the ELC_GPTF input	R/W*1
22	PSELCG	ELC_GPTG Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTG input 1: Counter stop enabled at the ELC_GPTG input	R/W*1
23	PSELCH	ELC_GPTH Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTH input 1: Counter stop enabled at the ELC_GPTH input	R/W*1
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTOP	Software Source Counter Stop Enable 0: Counter stop disabled by the GTSTP register 1: Counter stop enabled by the GTSTP register	R/W*1

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

The GTPSR sets the source to stop the GTCNT counter.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGB pin input.

PSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Stop Enable)

PSGTRGCR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGC pin input.

PSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Stop Enable)

The PSGTRGCF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGC pin input.

PSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Stop Enable)

PSGTRGDR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGD pin input.

PSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Stop Enable)

The PSGTRGDF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGD pin input.

PSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

PSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCARBH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

PSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

PSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

PSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

PSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

PSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

PSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

PSELCm bit (ELCm Event Source Counter Stop Enable) (m = A to H)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by the GTSTP register.

23.2.7 GTCSR : General PWM Timer Clear Source Select Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	CP1CCE	CSCMSC[2:0]			CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTETRGA input 1: Counter clear enabled on the rising edge of GTETRGA input	R/W*1
1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGA input 1: Counter clear enabled on the falling edge of GTETRGA input	R/W*1
2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGB input 1: Enable counter clear on the rising edge of GTETRGB input	R/W*1
3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGB input 1: Counter clear enabled on the falling edge of GTETRGB input	R/W*1
4	CSGTRGCR	GTETRGC Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGC input 1: Enable counter clear on the rising edge of GTETRGC input	R/W*1
5	CSGTRGCF	GTETRGC Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGC input 1: Counter clear enabled on the falling edge of GTETRGC input	R/W*1
6	CSGTRGDR	GTETRGD Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGD input 1: Enable counter clear on the rising edge of GTETRGD input	R/W*1
7	CSGTRGDF	GTETRGD Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGD input 1: Counter clear enabled on the falling edge of GTETRGD input	R/W*1
8	CSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	CSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	CSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	CSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	CSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	CSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	CSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W

Bit	Symbol	Function	R/W
15	CSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	CSELCA	ELC_GPTA Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTA input 1: Counter clear enabled at the ELC_GPTA input	R/W*1
17	CSELCB	ELC_GPTB Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTB input 1: Counter clear enabled at the ELC_GPTB input	R/W*1
18	CSELCC	ELC_GPTC Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTC input 1: Counter clear enabled at the ELC_GPTC input	R/W*1
19	CSELCD	ELC_GPTD Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTD input 1: Counter clear enabled at the ELC_GPTD input	R/W*1
20	CSELCE	ELC_GPTE Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTE input 1: Counter clear enabled at the ELC_GPTE input	R/W*1
21	CSELCF	ELC_GPTF Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTF input 1: Counter clear enabled at the ELC_GPTF input	R/W*1
22	CSELCG	ELC_GPTG Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTG input 1: Counter clear enabled at the ELC_GPTG input	R/W*1
23	CSELCH	ELC_GPTH Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTH input 1: Counter clear enabled at the ELC_GPTH input	R/W*1
26:24	CSCMSC[2:0]	Compare Match/Input Capture/Synchronous counter clearing Source Counter Clear Enable*2 0 0 0: Counter clear disabled by Compare match/ Input capture/ Synchronous counter clearing group 0 0 1: Counter clear enabled at the GTCCRA register compare match/ Input capture 0 1 0: Counter clear enabled at the GTCCRB register compare match/ Input capture 0 1 1: Counter clear enabled at the GTCCRC register compare match 1 0 0: Counter clear enabled at the GTCCRD register compare match 1 0 1: Counter clear enabled at the GTCCRE register compare match 1 1 0: Counter clear enabled at the GTCCRF register compare match 1 1 1: Counter clear enabled at the synchronous counter clearing group	R/W
27	CP1CCE	Complementary PWM mode1 Crest Source Counter Clear Enable*2 0: Counter clear disabled at the crest of complementary PWM mode1 1: Counter clear enabled at the crest of complementary PWM mode1	R/W*1
30:28	—	These bits are read as 0. The write value should be 0.	R/W
31	CCLR	Software Source Counter Clear Enable 0: Counter clear disabled by the GTCLR register 1: Counter clear enabled by the GTCLR register	R/W*1

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.
Note 2. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.

The GTCSR sets the source to clear the GTCNT counter.

Counter clearing can be executed whether the counter is running (GTCR.CST=1) or stopped (GTCR.CST=0).

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGB pin input.

CSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Clear Enable)

The CSGTRGCR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGC pin input.

CSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Clear Enable)

The CSGTRGCF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGC pin input.

CSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Clear Enable)

The CSGTRGDR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGD pin input.

CSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Clear Enable)

The CSGTRGDF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGD pin input.

CSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

CSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

CSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

In complementary PWM mode, this setting is invalid.

CSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

In complementary PWM mode, this setting is invalid.

CSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

CSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

CSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

In complementary PWM mode, this setting is invalid.

CSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

In complementary PWM mode, this setting is invalid.

CSELCm bit (ELCm Event Source Counter Clear Enable) (m = A to H)

The CSELCm bit enables or disables the GTCNT counter clear at the ELC_GPTm event input.

CSCMSC[2:0] bit (Compare Match/Input Capture/Synchronous counter clearing Source Counter Clear Enable*2)

Select enable or disable for the counter clear of the GTCNT counter by compare match/input capture/synchronous counter clearing group.

Since the compare match by the register that is performing the buffer operation (including the wave mode specific case) does not occur, the counter clear enable setting that makes the target register of the buffer operation the compare match factor is invalid.

In complementary PWM mode, the counter clear enable setting for compare match of the GTCCRB register, GTCCRE register, and GTCCRF register is invalid even when the buffer operation is not performed.

CP1CCE bit (Complementary PWM mode1 Crest Source Counter Clear Enable)

Select enable or disable for the counter clear at the crest of complementary PWM mode 1.

To enable this bit, do not set 1 to the PSYE bit of the GTIOR register.

It is valid only for the master channel in complementary PWM mode. The master channel setting also clears the GTCNT counter of the slave channel in complementary PWM mode.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables the GTCNT counter clear by the GTCLR register.

23.2.8 GTUPSR : General PWM Timer Up Count Source Select Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	USILVL[3:0]				USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGA input 1: Counter count up enabled on the rising edge of GTETRGA input	R/W

Bit	Symbol	Function	R/W
1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGA input 1: Counter count up enabled on the falling edge of GTETRGA input	R/W
2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGB input 1: Counter count up enabled on the rising edge of GTETRGB input	R/W
3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGB input 1: Counter count up enabled on the falling edge of GTETRGB input	R/W
4	USGTRGCR	GTETRGC Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGC input 1: Counter count up enabled on the rising edge of GTETRGC input	R/W
5	USGTRGCF	GTETRGC Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGC input 1: Counter count up enabled on the falling edge of GTETRGC input	R/W
6	USGTRGDR	GTETRGD Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGD input 1: Counter count up enabled on the rising edge of GTETRGD input	R/W
7	USGTRGDF	GTETRGD Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGD input 1: Counter count up enabled on the falling edge of GTETRGD input	R/W
8	USCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	USCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	USCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	USCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	USCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	USCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	USCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W

Bit	Symbol	Function	R/W
15	USCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	USELCA	ELC_GPTA Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTA input 1: Counter count up enabled at the ELC_GPTA input	R/W
17	USELCB	ELC_GPTB Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTB input 1: Counter count up enabled at the ELC_GPTB input	R/W
18	USELCC	ELC_GPTC Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTC input 1: Counter count up enabled at the ELC_GPTC input	R/W
19	USELCD	ELC_GPTD Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTD input 1: Counter count up enabled at the ELC_GPTD input	R/W
20	USELCE	ELC_GPTE Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTE input 1: Counter count up enabled at the ELC_GPTE input	R/W
21	USELCF	ELC_GPTF Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTF input 1: Counter count up enabled at the ELC_GPTF input	R/W
22	USELCG	ELC_GPTG Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTG input 1: Counter count up enabled at the ELC_GPTG input	R/W
23	USELCH	ELC_GPTH Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTH input 1: Counter count up enabled at the ELC_GPTH input	R/W
27:24	USILVL[3:0]	External Input Level Source Count-Up Enable 0 0 0 0: Disables count-up by external input level 0 0 0 1: Setting prohibited 0 0 1 0: Enables count-up by GTIOCnA pin input level 0 0 0 1 1: Enables count-up by GTIOCnA pin input level 1 0 1 0 0: Enables count-up by GTIOCnB pin input level 0 0 1 0 1: Enables count-up by GTIOCnB pin input level 1 0 1 1 0: Setting prohibited 0 1 1 1: Setting prohibited 1 0 0 0: Enables count-up by GTETRGA pin input level 0 1 0 0 1: Enables count-up by GTETRGA pin input level 1 1 0 1 0: Enables count-up by GTETRGB pin input level 0 1 0 1 1: Enables count-up by GTETRGB pin input level 1 1 1 0 0: Enables count-up by GTETRGC pin input level 0 1 1 0 1: Enables count-up by GTETRGC pin input level 1 1 1 1 0: Enables count-up by GTETRGD pin input level 0 1 1 1 1: Enables count-up by GTETRGD pin input level 1	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTUPSR sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Number of increment in counting is one even when multiple sources are generated simultaneously.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGB pin input.

USGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Up Enable)

The USGTRGCR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGC pin input.

USGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Up Enable)

The USGTRGCF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGC pin input.

USGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Up Enable)

The USGTRGDR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGD pin input.

USGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Up Enable)

The USGTRGDF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGD pin input.

USCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables GTCNT counter count up on the rising edge of GTIOCnA pin input, when GTIOCnB input is 0.

USCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

USCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

USCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

USCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to H)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

USILVL[3:0] bit (External Input Level Source Count-Up Enable)

Select enable or disable for the count-up of the GTCNT counter by the GTIOCnA pin input level, GTIOCnB pin input level, and GTETRGA/GTETRGB/GTETRGC/GTETRGD input level.

23.2.9 GTDNSR : General PWM Timer Down Count Source Select Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	DSILVL[3:0]				DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGA input 1: Counter count down enabled on the rising edge of GTETRGA input	R/W
1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGA input 1: Counter count down enabled on the falling edge of GTETRGA input	R/W
2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGB input 1: Counter count down enabled on the rising edge of GTETRGB input	R/W
3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGB input 1: Counter count down enabled on the falling edge of GTETRGB input	R/W
4	DSGTRGCR	GTETRGC Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGC input 1: Counter count down enabled on the rising edge of GTETRGC input	R/W
5	DSGTRGCF	GTETRGC Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGC input 1: Counter count down enabled on the falling edge of GTETRGC input	R/W
6	DSGTRGDR	GTETRGD Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGD input 1: Counter count down enabled on the rising edge of GTETRGD input	R/W
7	DSGTRGDF	GTETRGD Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGD input 1: Counter count down enabled on the falling edge of GTETRGD input	R/W
8	DSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	DSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W

Bit	Symbol	Function	R/W
10	DSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	DSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	DSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	DSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	DSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	DSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTA input 1: Counter count down enabled at the ELC_GPTA input	R/W
17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTB input 1: Counter count down enabled at the ELC_GPTB input	R/W
18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTC input 1: Counter count down enabled at the ELC_GPTC input	R/W
19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTD input 1: Counter count down enabled at the ELC_GPTD input	R/W
20	DSELCE	ELC_GPTE Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTE input 1: Counter count down enabled at the ELC_GPTE input	R/W
21	DSELCF	ELC_GPTF Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input	R/W
22	DSELCG	ELC_GPTG Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTG input 1: Counter count down enabled at the ELC_GPTG input	R/W

Bit	Symbol	Function	R/W
23	DSELCH	ELC_GPTF Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input	R/W
27:24	DSILVL[3:0]	External Input Level Source Count-Down Enable 0 0 0 0: Disables count-down by external input level 0 0 0 1: Setting prohibited 0 0 1 0: Enables count-down by GTIOCnA pin input level 0 0 0 1 1: Enables count-down by GTIOCnA pin input level 1 0 1 0 0: Enables count-down by GTIOCnB pin input level 0 0 1 0 1: Enables count-down by GTIOCnB pin input level 1 0 1 1 0: Setting prohibited 0 1 1 1: Setting prohibited 1 0 0 0: Enables count-down by GTETRGA pin input level 0 1 0 0 1: Enables count-down by GTETRGA pin input level 1 1 0 1 0: Enables count-down by GTETRGB pin input level 0 1 0 1 1: Enables count-down by GTETRGB pin input level 1 1 1 0 0: Enables count-down by GTETRGC pin input level 0 1 1 0 1: Enables count-down by GTETRGC pin input level 1 1 1 1 0: Enables count-down by GTETRGD pin input level 0 1 1 1 1: Enables count-down by GTETRGD pin input level 1	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTDNSR sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted down by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Number of decrement in counting is one even when multiple sources are generated simultaneously.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGB pin input.

DSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Down Enable)

The DSGTRGCR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGC pin input.

DSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Down Enable)

The DSGTRGCF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGC pin input.

DSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Down Enable)

The DSGTRGDR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGD pin input.

DSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Down Enable)

The DSGTRGDF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGD pin input.

DSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

DSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

DSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCnB pin input, when GTIOCnA input is 1.

DSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to H)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

DSILVL[3:0] bit (External Input Level Source Count-Down Enable)

Select enable or disable for the count-down of the GTCNT counter by the GTIOCnA pin input level, GTIOCnB pin input level, and GTETRGA/GTETRGB/GTETRGC/GTETRGD input level.

23.2.10 GTICASR : General PWM Timer Input Capture Source Select Register A

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	ASOC	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGA input 1: GTCCRA input capture enabled on the rising edge of GTETRGA input	R/W
1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGA input 1: GTCCRA input capture enabled on the falling edge of GTETRGA input	R/W
2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGB input 1: GTCCRA input capture enabled on the rising edge of GTETRGB input	R/W
3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGB input 1: GTCCRA input capture enabled on the falling edge of GTETRGB input	R/W
4	ASGTRGCR	GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGC input 1: GTCCRA input capture enabled on the rising edge of GTETRGC input	R/W
5	ASGTRGCF	GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGC input 1: GTCCRA input capture enabled on the falling edge of GTETRGC input	R/W
6	ASGTRGDR	GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGD input 1: GTCCRA input capture enabled on the rising edge of GTETRGD input	R/W
7	ASGTRGDF	GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGD input 1: GTCCRA input capture enabled on the falling edge of GTETRGD input	R/W
8	ASCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	ASCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	ASCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W

Bit	Symbol	Function	R/W
11	ASCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	ASCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	ASCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	ASCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	ASCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTA input 1: GTCCRA input capture enabled at the ELC_GPTA input	R/W
17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTB input 1: GTCCRA input capture enabled at the ELC_GPTB input	R/W
18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTC input 1: GTCCRA input capture enabled at the ELC_GPTC input	R/W
19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTD input 1: GTCCRA input capture enabled at the ELC_GPTD input	R/W
20	ASELCE	ELC_GPTE Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTE input 1: GTCCRA input capture enabled at the ELC_GPTE input	R/W
21	ASELCF	ELC_GPTF Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTF input 1: GTCCRA input capture enabled at the ELC_GPTF input	R/W
22	ASELCG	ELC_GPTG Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTG input 1: GTCCRA input capture enabled at the ELC_GPTG input	R/W
23	ASELCH	ELC_GPTH Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTH input 1: GTCCRA input capture enabled at the ELC_GPTH input	R/W
24	ASOC	Other channel Source GTCCRA Input Capture Enable*1 0: Disables GTCCRA input capture by other channel factor 1: Enables GTCCRA input capture by other channel factor	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is only available in GPT324 to GPT329.

In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.

The GTICASR sets the source of input capture for GTCCRA.

When at least one bit among bits in the GTICASR register is set to 1, input capture operation making the GTCCRA register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGA pin input.

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGB pin input.

ASGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGCR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGC pin input.

ASGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGCF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGC pin input.

ASGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGDR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGD pin input.

ASGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGDF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGD pin input.

ASCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

ASCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when the GTIOCnB input is 1.

ASCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

ASCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

ASCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to H)

The ASELCm bit enables or disables the input capture for GTCCRA at the ELC_GPTm event input.

ASOC bit (Other channel Source GTCCRA Input Capture Enable)

Select enable or disable for an input capture to the GTCCRA register by other channel factor.

Input capture of other channel factors is not subject to input capture factors to other channels set by the ICAFA and ICBFA bits of the GTICCR register.

23.2.11 GTICBSR : General PWM Timer Input Capture Source Select Register B

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	BSOC	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGA input 1: GTCCRB input capture enabled on the rising edge of GTETRGA input	R/W
1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGA input 1: GTCCRB input capture enabled on the falling edge of GTETRGA input	R/W
2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGB input 1: GTCCRB input capture enabled on the rising edge of GTETRGB input	R/W
3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGB input 1: GTCCRB input capture enabled on the falling edge of GTETRGB input	R/W
4	BSGTRGCR	GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGC input 1: GTCCRB input capture enabled on the rising edge of GTETRGC input	R/W

Bit	Symbol	Function	R/W
5	BSGTRGCF	GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGC input 1: GTCCRB input capture enabled on the falling edge of GTETRGC input	R/W
6	BSGTRGDR	GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGD input 1: GTCCRB input capture enabled on the rising edge of GTETRGD input	R/W
7	BSGTRGDF	GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGD input 1: GTCCRB input capture enabled on the falling edge of GTETRGD input	R/W
8	BSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	BSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	BSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	BSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	BSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	BSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	BSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	BSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTA input 1: GTCCRB input capture enabled at the ELC_GPTA input	R/W

Bit	Symbol	Function	R/W
17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTB input 1: GTCCRB input capture enabled at the ELC_GPTB input	R/W
18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTC input 1: GTCCRB input capture enabled at the ELC_GPTC input	R/W
19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTD input 1: GTCCRB input capture enabled at the ELC_GPTD input	R/W
20	BSELCE	ELC_GPTE Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTE input 1: GTCCRB input capture enabled at the ELC_GPTE input	R/W
21	BSELCF	ELC_GPTF Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTF input 1: GTCCRB input capture enabled at the ELC_GPTF input	R/W
22	BSELCG	ELC_GPTG Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTG input 1: GTCCRB input capture enabled at the ELC_GPTG input	R/W
23	BSELCH	ELC_GPTH Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTH input 1: GTCCRB input capture enabled at the ELC_GPTH input	R/W
24	BSOC	Other channel Source GTCCRB Input Capture Enable*1 0: Disables GTCCRB input capture by other channel factor 1: Enables GTCCRB input capture by other channel factor	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.

The GTICBSR sets the source of input capture for GTCCRB.

When at least one bit among bits in the GTICBSR register is set to 1, input capture operation making the GTCCRB register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT through the POEG. Set the polarity of these signals with the POEG.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables the input capture for GTCCRB on the rising edge of the GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGB pin input.

BSGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGCR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGC pin input.

BSGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGCF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGC pin input.

BSGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGDR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGD pin input.

BSGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGDF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGD pin input.

BSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

BSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

BSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to H)

The BSELCm bit enables or disables the input capture for GTCCRB at the ELC_GPTm event input.

BSOC bit (Other channel Source GTCCRB Input Capture Enable)

Select enable or disable for an input capture to the GTCCRB register by other channel factor.

Input capture of other channel factors is not subject to input capture factors to other channels set by the ICAFB and ICBFB bits of the GTICCR register.

23.2.12 GTCR : General PWM Timer Control Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CKEG[1:0]		TPCS[3:0]				—	—	—	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCEN	—	—	CPSCD	SSCGRP[1:0]		SCGTIOC	ICDS	—	—	BINV	AINV	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	Count Start 0: Count operation is stopped 1: Count operation is performed	R/W*1
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	AINV	GTIOCnA input/output pin polarity reversal control 0: Not invert 1: Invert	R/W
5	BINV	GTIOCnB input/output pin polarity reversal control 0: Not invert 1: Invert	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	ICDS	Input Capture Operation Select During Count Stop 0: Input capture is operated during count stop. 1: Input capture is not operated during count stop.	R/W
9	SCGTIOC	GTIOC input Source Synchronous Clear Enable*2 0: Disables to use the counter clear by GTIOC input as the clear factor for other channels 1: Enables to use the counter clear by GTIOC input as the clear factor for other channels	R/W
11:10	SSCGRP[1:0]	Synchronous Set/Clear Group Select*2 0 0: Select synchronous set/clear group A 0 1: Select synchronous set/clear group B 1 0: Select synchronous set/clear group C 1 1: Select synchronous set/clear group D	R/W*1
12	CPSCD	Complementary PWM Mode Synchronous Clear Disable*2 0: Enable synchronous counter clear by other channel other than the section of trough in complementary PWM mode 1: Disable synchronous counter clear by other channel other than the section of trough in complementary PWM mode	R/W*1
14:13	—	These bits are read as 0. The write value should be 0.	R/W
15	SSCEN	Synchronous Set/Clear Enable*2 0: Disable Synchronous set/clear of the GTCNT counter 1: Enable Synchronous set/clear of the GTCNT counter	R/W*1

Bit	Symbol	Function	R/W
19:16	MD[3:0]	Mode Select*3 0 0 0 0: Saw-wave PWM mode 1 (single buffer or double buffer possible) 0 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 0 1 0: Saw-wave PWM mode 2 (single buffer or double buffer possible) 0 0 1 1: Setting prohibited 0 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 0 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 0 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 0 1 1 1: Setting prohibited 1 0 0 0: Setting prohibited 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: Complementary PWM mode 1 (transfer at crest) 1 1 0 1: Complementary PWM mode 2 (transfer at trough) 1 1 1 0: Complementary PWM mode 3 (transfer at crest and trough) 1 1 1 1: Complementary PWM mode 4 (immediate transfer)	R/W*1
22:20	—	These bits are read as 0. The write value should be 0.	R/W
26:23	TPCS[3:0]	Timer Prescaler Select 0 0 0 0: GTCLK/1 0 0 0 1: GTCLK/2 0 0 1 0: GTCLK/4 0 0 1 1: GTCLK/8 0 1 0 0: GTCLK/16 0 1 0 1: GTCLK/32 0 1 1 0: GTCLK/64 0 1 1 1: GTCLK/128 1 0 0 0: GTCLK/256 1 0 0 1: GTCLK/512 1 0 1 0: GTCLK/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (Via the POEG) 1 1 0 1: GTETRGB (Via the POEG) 1 1 1 0: GTETRGC (Via the POEG) 1 1 1 1: GTETRGD (Via the POEG)	R/W*1
28:27	CKEG[1:0]	Clock Edge Select 0 0: Select rising edge of GTETRG for clock count 0 1: Select falling edge of GTETRG for clock count Others: Select both edge of GTETRG for clock count	R/W*1
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.
Note 2. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.
Note 3. MD[3] bit is only available in GPT324 to GPT329. GPT320 to GPT323 and GPT3210 to GPT3213 only support Saw-wave PWM mode and Triangle-wave PWM mode except Saw-wave PWM mode 2.

The GTCR controls GTCNT.

Access in 8 bit unit to GTCR is prohibited.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- The GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input that are enabled by GTSSR for the starting counter source, occurs (n = 0 to 13)
- 1 is written by software directly.

[Clearing conditions]

- The GTSTP value where the channel number associated with the bit number is set to 1 with the GTPSR.CSTOP bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input enabled by GTPSR as the counter stop source, occurs (n = 0 to 13)
- 0 is written by software directly.
- When the period count function is finished while the GTPC.ASTP bit is (n = 0 to 3, 10 to 13).

AINV bit (GTIOCnA input/output pin polarity reversal control)

This bit selects GTIOCnA input/output pin polarity reversal control.

BINV bit (GTIOCnB input/output pin polarity reversal control)

This bit selects GTIOCnB input/output pin polarity reversal control.

ICDS bit (Input Capture Operation Select During Count Stop)

This bit selects input capture operation during count stop, when the input capture function is selected.

SCGTIOC bit (GTIOC input Source Synchronous Clear Enable)

Select enable or disable the use of the counter clear by GTIOCnA/GTIOCnB input pin selected by the GTCSR register as the counter clear factor for other channels.

SSCGRP[1:0] bits (Synchronous Set/Clear Group Select)

Select the channel group of synchronous set/clear.

In complementary PWM mode, slave channels are also controlled by setting the SSCGRP[1:0] bits of the master channel.

CPSCD bit (Complementary PWM Mode Synchronous Clear Disable)

Select disable or enable of counter clear when synchronous clear from other channel occurs except section of trough in complementary PWM mode.

The slave channel is also controlled by setting the CPSCD bit of the master channel.

SSCEN bit (Synchronous Set/Clear Enable)

Select disable or enable of Synchronous set/clear.

In complementary PWM mode, slave channels are also controlled by setting the SSCEN bits of the master channel.

MD[3:0] bits (Mode Select)

These bits select the GPT operating mode.

In complementary PWM mode, slave channels are also controlled by setting the MD bits of the master channel.

Only the MD[3:2] bit (MD[2] for GPT320 to GPT323) is valid at input capture. Counting in saw-wave mode is performed with 00 for the MD[3:2] bit (0 for the MD[2] of GPT320 to GPT323), and counting in triangle-wave mode is performed with 01 for the MD[3:2] bit (1 for MD[2] of GPT320 to GPT323), and counting in complementary PWM mode is performed with 1 for the MD[3].

The MD bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave or complementary PWM modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

TPCS[3:0] bits (Timer Prescaler Select)

The TPCS[3:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[3:0] bits must be set while the GTCNT operation is stopped.

CKEG[1:0] bits (Clock Edge Select)

When GTETRG input is selected by TPCS[3:0] bits, select the edge of GTETRG input used as the clock of GTCNT counter.

Set the CKEG[1:0] bits only when the GTCNT counter operation is stopped.

23.2.13 GTUDDTYC : General PWM Timer Count Direction and Duty Setting Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	OABDTYT	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	Count Direction Setting 0: GTCNT counts down 1: GTCNT counts up	R/W
1	UDF	Forcible Count Direction Setting 0: Not forcibly set 1: Forcibly set	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
17:16	OADTY[1:0]	GTIOCnA Output Duty Setting 0 0: GTIOCnA pin duty depends on the compare match 0 1: GTIOCnA pin duty depends on the compare match 1 0: GTIOCnA pin duty 0% 1 1: GTIOCnA pin duty 100%	R/W
18	OADTYF	Forcible GTIOCnA Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
19	OADTYR	GTIOCnA Output Value Selecting after Releasing 0%/100% Duty Setting 0: The function selected by the GTIOA[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOA[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	OBDTY[1:0]	GTIOCnB Output Duty Setting 0 0: GTIOCnB pin duty depends on the compare match 0 1: GTIOCnB pin duty depends on the compare match 1 0: GTIOCnB pin duty 0% 1 1: GTIOCnB pin duty 100%	R/W
26	OBDTYF	Forcible GTIOCnB Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
27	OBDTYR	GTIOCnB Output Value Selecting after Releasing 0%/100% Duty Setting 0: The function selected by the GTIOB[3:2] bits is applied to the output value when the duty cycle is set after release from the 0 or 100% duty-cycle setting. 1: The function selected by the GTIOB[3:2] bits is applied to the compare match output value which is masked after release from the 0 or 100% duty-cycle setting.	R/W
28	OABDTYT	GTIOCnA, B pin output 0%/100% duty setting reflection timing setting 0: The output duty-cycle setting changed at an underflow is reflected. 1: The output duty-cycle setting changed at an underflow and at the top of triangle-wave is reflected. The setting value “1” is invalid except the triangle-wave PWM mode.	R/W

Bit	Symbol	Function	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

The GTUDDTYC sets the direction in which the GTCNT counts (up-counting or down-counting), and sets the duty of the GTIOCnA/GTIOCnB pin output.

The setting is invalid during the event count operation, Saw-wave PWM mode 2, Complementary PWM mode.

Count Direction:

- In saw-wave mode.
  When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting stops, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UDF bit is set to 1 while counting stops, the UD bit value is reflected in the count direction when counting starts.
- In triangle-wave mode.
  When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.
  When the UDF bit is set to 1 while counting is stopped, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only 0 should be written to this bit during counter operation. When 1 is written to this bit while counting stops, return this bit to 0 before counting starts.

Output duty

- In saw-wave mode.
  When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR).
  When the OADTY/OBDTY value is changed during down-counting, the duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.
- In triangle-wave mode.
  When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.

In both saw-wave mode and triangle-wave mode, when the OADTYF/OBDTYF bit is set back to 0 and the OADTY[1:0]/OBDTY[1:0] bits are set after setting the OADTYF/OBDTYF bit to 1 and setting the OADTY[1:0]/OBDTY[1:0] bits for the duty of first cycle while count operation is stopped, these duty-cycle set during stopping count operation are reflected in the first cycle and the second cycle after starting count operation.

OmDTY[1:0] bits (GTIOCnm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty (0%, 100% or compare match control) of the GTIOCnm pin.

OmDTYF bit (Forcible GTIOCnm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. Set this bit to 0 during counter operation.

OmDTYR bit (GTIOCnm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

The OmDTYR bit selects the value that is the object of output retained or toggled at cycle end, when the control changes from 0% or 100% duty setting to compare match for the GTIOCnm pin and GTIOR.GTIOm[3:2] bits are set to 00b (output retained at cycle end) or the GTIOR.GTIOm[3:2] bits are set to 11b (output toggled at cycle end).

The GPT internally continues to perform compare match operation during duty-cycle 0% or 100% operation. When the OmDTYR bit is 1, the value after the period has elapsed due this compare match operation is target for the GTIOm[3:2] bits.

OABDTYT Bit (GTIOCnm pin output 0%/100% duty setting reflection timing setting) (n = 0 − (value of P_NUMCHALL − 1), m = A, B)

Select the reflection timing of the 0%/100% duty setting for the GTIOCnm pin in triangle-wave mode.

If the OABDTYT bit is 0, the output duty setting set in the GTUDDTYC.OADTY[1:0] and OBDTY[1:0] bits is reflected when an underflow occurs.

If the OABDTYT bit is “1”, the output duty setting set in the GTUDDTYC.OADTY[1:0] and OBDTY[1:0] bits is reflected when underflow occurs and at the top of the triangle-wave.

23.2.14 GTIOR : General PWM Timer I/O Control Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	OBEOCD	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	PSYE	OAEOCD	OADF[1:0]		OAE	OAHLD	OADFLT	CPSCIR	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA Pin Function Select See Table 23.4 and Table 23.5.	R/W
5	CPSCIR*1	Complementary PWM Mode Initial Output at Synchronous Clear Disable 0: Output the initial value set by the GTIOR.GTIOA and GTIOB bits when synchronous clear occurs in Trough section of complementary PWM mode 1: Disable output the initial value	R/W
6	OADFLT	GTIOCnA Pin Output Value Setting at the Count Stop 0: The GTIOCnA pin outputs low when counting stops 1: The GTIOCnA pin outputs high when counting stops	R/W
7	OAHLD	GTIOCnA Pin Output Setting at the Start/Stop Count 0: The GTIOCnA pin output level at the start or stop of counting depends on the register setting 1: The GTIOCnA pin output level is retained at the start or stop of counting	R/W
8	OAE	GTIOCnA Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W

Bit	Symbol	Function	R/W
10:9	OADF[1:0]	GTIOCnA Pin Disable Value Setting 0 0: None of the below options are specified 0 1: GTIOCnA pin is set to Hi-Z in response to controlling the output negation 1 0: GTIOCnA pin is set to 0 in response to controlling the output negation 1 1: GTIOCnA pin is set to 1 in response to controlling the output negation	R/W
11	OAEOCD[*1]	GTCCRA Compare Match Cycle End Output Invalidate 0: Validate GTIOA[3:2] setting 1: Invalidate GTIOA[3:2] setting (GTIOCnA pin output is retained)	R/W
12	PSYE	PWM Synchronous output Enable 0: Disable GTCPPOm pin output 1: Enable GTCPPOm pin output	R/W
13	NFAEN	Noise Filter A Enable 0: The noise filter for the GTIOCnA pin is disabled 1: The noise filter for the GTIOCnA pin is enabled	R/W
15:14	NFCSA[1:0]	Noise Filter A Sampling Clock Select 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W
20:16	GTIOB[4:0]	GTIOCnB Pin Function Select See Table 23.4 and Table 23.5.	R/W
21	—	This bit is read as 0. The write value should be 0.	R/W
22	OBDFLT	GTIOCnB Pin Output Value Setting at the Count Stop 0: The GTIOCnB pin outputs low when counting stops 1: The GTIOCnB pin outputs high when counting stops	R/W
23	OBHLD	GTIOCnB Pin Output Setting at the Start/Stop Count 0: The GTIOCnB pin output level at the start/stop of counting depends on the register setting 1: The GTIOCnB pin output level is retained at the start/stop of counting	R/W
24	OBE	GTIOCnB Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
26:25	OBDF[1:0]	GTIOCnB Pin Disable Value Setting 0 0: None of the below options are specified 0 1: GTIOCnB pin is set to Hi-Z in response to controlling the output negation 1 0: GTIOCnB pin is set to 0 in response to controlling the output negation 1 1: GTIOCnB pin is set to 1 in response to controlling the output negation	R/W
27	OBEOCD[*1]	GTCCRB Compare Match Cycle End Output Invalidate 0: When Saw-wave PWM mode 1, validate GTIOB[3:2] setting When Saw-wave PWM mode 2, validate GTIOA[3:2] setting 1: When Saw-wave PWM mode 1, invalidate GTIOB[3:2] setting (GTIOCnB pin output is retained) When Saw-wave PWM mode 2, invalidate GTIOA[3:2] setting (GTIOCnA pin output is retained)	R/W
28	—	This bit is read as 0. The write value should be 0.	R/W
29	NFBEN	Noise Filter B Enable 0: The noise filter for the GTIOCnB pin is disabled 1: The noise filter for the GTIOCnB pin is enabled	R/W
31:30	NFCSB[1:0]	Noise Filter B Sampling Clock Select 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W

Note 1. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.

The GTIOR sets the functions of the GTIOCnA, GTIOCnB and GTCPPOm pins. (n = 0 to 13, m = 0 to 13)

GTIOA[4:0] bits (GTIOCnA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCnA pin function. For details, see Table 23.4 and Table 23.5.

CPSCIR bit (Complementary PWM Mode Initial Output at Synchronous Clear Disable)

Select the output waveform when synchronous clear occurs in complementary PWM mode.

The initial output is disabled by this function only when synchronous clear occurs in the trough section in complementary PWM mode. If a synchronous clear occurs at any other time, the initial value set by the GTIOA[4]/GTIOB[4] bits is output regardless of the CPSCIR bit setting. In addition, the initial value set by the GTIOA[4]/GTIOB[4] bits is output even when the synchronous clear occurs in the trough section immediately after the count starts.

OADFLT bit (GTIOCnA Pin Output Value Setting at the Count Stop)

The OADFLT bit sets whether the GTIOCnA pin outputs high or low when counting stops.

OAHLD bit (GTIOCnA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCnA pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OAHLD bit is set to 0:

- The value specified in bit [4] of the GTIOA[4:0] bits is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OAHLD bit is set to 1:

- The output is retained when counting starts or stops.

OAE bit (GTIOCnA Pin Output Enable)

The OAE bit disables or enables the GTIOCnA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCnA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCnA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCnA pin in response to a request to disable output from the POEG.

OAEOCD bit (GTCCRA Compare Match Cycle End Output Invalidate)

If the cycle end matches the GTCCRA compare match timing in Saw-wave PWM mode 1 and 2, select invalid/valid of the setting of GTIOA[3:2] bits. When 1 (disabled) is set, the GTIOCnA pin holds the output when the cycle end and the GTCCRA compare match timing match.

PSYE bit (PWM Synchronous output Enable)

This bit set Enable/disable of output signal from GTCPPOm pin synchronized with the PWM cycle that toggles at the crest/trough/GTCNT counter clear of complementary PWM mode and Triangle-wave mode or the end of the cycle of the Saw-wave mode.

The initial output of the GTCPPOn output pin is Low, and the count start results in High.

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCnA pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCnA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCnB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCnB pin function. For details, see Table 23.4 and Table 23.5.

In Saw-wave PWM mode 2, only the GTIOB[1:0] bits are valid, and the GTIOCnA pin output is selected instead of the GTIOCnB pin by the GTCCRB register compare match.

OBDFLT bit (GTIOCnB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCnB pin outputs high or low when counting stops.

OBHLD bit (GTIOCnB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether the GTIOCnB pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCnB Pin Output Enable)

The OBE bit disables or enables the GTIOCnB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCnB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCnB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCnB pin in response to a request to disable output from the POEG.

OBEOCD bit (GTCCRB Compare Match Cycle End Output Invalidate)

If the cycle end matches the GTCCRB compare match timing in Saw-wave PWM mode 1 and 2, select invalid/valid of the GTIOB[3:2] bits setting in saw-wave PWM mode 1 or the GTIOA[3:2] bit setting in saw-wave PWM mode 2. When 1 (disabled) is set, the GTIOCnB pin in saw-wave PWM mode 1 or the GTIOCnA pin in saw-wave PWM mode 2 holds the output when the cycle end and the GTCCRB compare match timing match.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCnB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCnB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

Table 23.4 Settings of GTIOA[4:0] and GTIOB[4:0] bits (Saw-wave mode, Triangle-wave mode)

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4*4	b3, b2*1 *2 *3 *4	b1, b0*2
0	0	0	0	0	Initial output is low	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	0	0	0	Initial output is high	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting), an underflow (GTCNT changes from 0 to GTPR in down-counting), or counter clearing for saw-wave mode, and means a trough (GTCNT changes from 0 to 1) for triangle-wave mode.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, if the OAEOCD and OBEOCD bits are set to 0 and the end of cycle output is enabled, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

Note 4. In Saw-wave PWM mode 2, GTIOB[4:2] bits is invalid. Since only GTIOCnA pins are output pins, set GTIOA[4] bit for initial output. Set GTIOA[3:2] bits for output at the end of a cycle.

Table 23.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits (Complementary PWM mode)

GTIOA/GTIOB[4:0] bits*1 *2 *3					Function		
					Initial output, Active level	Up count Compare Match output	Down count Compare Match output
b4	b3	b2	b1	b0	b4	b3, b2	b1, b0
0	0	1	1	0	Initial output is Low. Active level is High.	Low output	High output
0	1	0	0	1		High output	Low output
1	0	1	1	0	Initial output is High. Active level is Low.	Low output	High output
1	1	0	0	1		High output	Low output

Note 1. In complementary PWM mode, the only values that can be set in the GTIOA[4:0] bits are 01001b, and 10110b. Setting other values is prohibited.

Note 2. In complementary PWM mode, the only values that can be set in the GTIOB[4:0] bits are 00110b, and 11001b. Setting other values is prohibited.

Note 3. In complementary PWM mode, setting GTIOB[4:0] bits does not use compare match of GTCCRB register. The combination of counter and register that is the target of compare match depends on the operation period of complementary PWM mode. For details, see section 23.3.3.7. Complementary PWM mode 1, 2, 3.

23.2.15 GTINTAD : General PWM Timer Interrupt Output Setting Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCFPU	SCFPO	SCFF	SCFE	SCFD	SCFC	SCFB	SCFA	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	SCFA	GTCCRA Register Compare Match/Input Capture Source Synchronous Clear Enable*1 0: Disable use of GTCCRA register compare match/input capture as a clear factor for other channels. 1: Enable use of GTCCRA register compare match/input capture as a clear factor for other channels.	R/W
9	SCFB	GTCCRB Register Compare Match/Input Capture Source Synchronous Clear Enable*1 0: Disable use of GTCCRB register compare match/input capture as a clear factor for other channels. 1: Enable use of GTCCRB register compare match/input capture as a clear factor for other channels.	R/W
10	SCFC	GTCCRC Register Compare Match Source Synchronous Clear Enable*1 0: Disable use of GTCCRC register compare match as a clear factor for other channels. 1: Enable use of GTCCRC register compare match as a clear factor for other channels.	R/W
11	SCFD	GTCCRD Register Compare Match Source Synchronous Clear Enable*1 0: Disable use of GTCCRD register compare match as a clear factor for other channels. 1: Enable use of GTCCRD register compare match as a clear factor for other channels.	R/W

Bit	Symbol	Function	R/W
12	SCFE	GTCCRE Register Compare Match Source Synchronous Clear Enable*1 0: Disable use of GTCCRE register compare match as a clear factor for other channels. 1: Enable use of GTCCRE register compare match as a clear factor for other channels	R/W
13	SCFF	GTCCRF Register Compare Match Source Synchronous Clear Enable*1 0: Disable use of GTCCRF register compare match as a clear factor for other channels. 1: Enable use of GTCCRF register compare match as a clear factor for other channels	R/W
14	SCFPO	Overflow Source Synchronous Clear Enable*1 0: Disable use of overflow as a clear factor for other channels. 1: Enable use of overflow as a clear factor for other channels.	R/W
15	SCFPU	Underflow Source Synchronous Clear Enable*1 0: Disable use of underflow as a clear factor for other channels 1: Enable use of underflow as a clear factor for other channels	R/W
16	ADTRAUEN	GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
17	ADTRADEN	GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
18	ADTRBUEN	GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
19	ADTRBDEN	GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Enable 0: A/D conversion start request is disabled. 1: A/D conversion start request is enabled.	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disable Source Select 0 0: Group A output disable source is selected 0 1: Group B output disable source is selected 1 0: Group C output disable source is selected 1 1: Group D output disable source is selected	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	GRPDTE	Dead Time Error Output Disable Request Enable 0: Dead time error output disable request is disabled. 1: Dead time error output disable request is enabled.	R/W
29	GRPABH	Same Time Output Level High Disable Request Enable 0: Same time output level high disable request disabled 1: Same time output level high disable request enabled	R/W
30	GRPABL	Same Time Output Level Low Disable Request Enable 0: Same time output level low disable request disabled 1: Same time output level low disable request enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.

The GTINTAD enables or disables interrupt requests, A/D conversion start request, and output disable requests.

SCFA bit (GTCCRA Register Compare Match/Input Capture Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRA register compare match/input capture as a clear factor for other channels.

SCFB bit (GTCCRB Register Compare Match/Input Capture Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRB register compare match/input capture as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFC bit (GTCCRC Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRC register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFD bit (GTCCRD Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRD register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFE bit (GTCCRE Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRE register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFF bit (GTCCRF Register Compare Match Source Synchronous Clear Enable)

This bit enables or disables use of GTCCRF register compare match as a clear factor for other channels.

The setting is invalid in complementary PWM mode.

SCFPO bit (Overflow Source Synchronous Clear Enable)

This bit enables or disables use of overflow as a clear factor for other channels.

In complementary PWM mode, it is valid only for the master channel.

SCFPU bit (Underflow Source Synchronous Clear Enable)

This bit enables or disables use of underflow as a clear factor for other channels.

In complementary PWM mode, it is valid only for the master channel.

ADTRAUEN bit (GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRA register compare matches during GTCNT counter up-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

ADTRADEN bit (GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRA register compare matches during GTCNT counter down-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

ADTRBUEN bit (GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRB register compare matches during GTCNT counter up-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

ADTRBDEN bit (GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Enable)

This bit enables or disables A/D conversion start requests generated by GTADTRB register compare matches during GTCNT counter down-counting.

In complementary PWM mode, it is valid only for the master channel.

The setting is invalid during the event count operation, and A/D conversion start request is not generated.

GRP[1:0] bits (Output Disable Source Select)

These bits select the group of output disable request from GPT to POEG and the group of output disable for GTIOCnA pin and GTIOCnB pin from POEG to GPT.

The output disable request to POEG is output to the group selected in the GRP[1:0] bit, with dead-time errors, simultaneous high output, and simultaneous low output factors following their respective disable request enable bits.

GTST.ODF shows the request of the output disable source group that is selected with the GRP[1:0] bits. Set the GRP[1:0] bits when both GTIOR.OAE and GTIOR.OBE bits are 0.

GRPDTE bit (Dead Time Error Output Disable Request Enable)

This bit enables or disables the output disable request by a dead time error.

The dead time error output disable request is not generated during the event count operation.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 0 at the same time.

23.2.16 GTST : General PWM Timer Status Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PCF	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	Input Capture/Compare Match Flag A 0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated	R/W*1
1	TCFB	Input Capture/Compare Match Flag B 0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated	R/W*1
2	TCFC	Input Compare Match Flag C 0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated	R/W*1
3	TCFD	Input Compare Match Flag D 0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated	R/W*1
4	TCFE	Input Compare Match Flag E 0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated	R/W*1

Bit	Symbol	Function	R/W
5	TCFF	Input Compare Match Flag F 0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated	R/W*1
6	TCFPO	Overflow Flag 0: No overflow (crest) occurred 1: An overflow (crest) occurred	R/W*1
7	TCFPU	Underflow Flag 0: No underflow (trough) occurred 1: An underflow (trough) occurred	R/W*1
10:8	ITCNT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter	R
14:11	—	These bits are read as 0. The write value should be 0.	R/W
15	TUCF	Count Direction Flag 0: GTCNT counter counts downward 1: GTCNT counter counts upward	R
16	ADTRAUF	GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Flag 0: No GTADTRA register compare match has occurred in up-counting. 1: A GTADTRA register compare match has occurred in up-counting.	R/W*1
17	ADTRADF	GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Flag 0: No GTADTRA register compare match has occurred in down-counting. 1: A GTADTRA register compare match has occurred in down-counting.	R/W*1
18	ADTRBUF	GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Flag 0: No GTADTRB register compare match has occurred in up-counting. 1: A GTADTRB register compare match has occurred in up-counting.	R/W*1
19	ADTRBDF	GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Flag 0: No GTADTRB register compare match has occurred in down-counting. 1: A GTADTRB register compare match has occurred in down-counting.	R/W*1
23:20	—	These bits are read as 0. The write value should be 0.	R/W
24	ODF	Output Disable Flag 0: No output disable request is generated 1: An output disable request is generated	R
27:25	—	These bits are read as 0. The write value should be 0.	R/W
28	DTEF	Dead Time Error Flag 0: No dead time error has occurred. 1: A dead time error has occurred.	R
29	OABHF	Same Time Output Level High Flag 0: No simultaneous generation of 1 both for the GTIOCA and GTIOCB pins has occurred. 1: A simultaneous generation of 1 both for the GTIOCA and GTIOCB pins has occurred.	R
30	OABLF	Same Time Output Level Low Flag 0: No simultaneous generation of 0 both for the GTIOCA and GTIOCB pins has occurred. 1: A simultaneous generation of 0 both for the GTIOCA and GTIOCB pins has occurred.	R
31	PCF*2	Period Count Function Finish Flag 0: No period count function finish has occurred 1: A period count function finish has occurred	R/W*1

Note 1. Only 0 can be written to this bit. Do not write 1.
When clearing the ADTRAUF, ADTRADF, ADTRBUF, or ADTRBDF flag, be sure to write 0 only to the target flag or flags for clearing and to write 1 to the other flags not for clearing.

Note 2. This bit is only available in GPT320 to GPT322 and GPT3210 to GPT3213.
In GPT324 to GPT329, this bit is read as 0. The write value should be 0.

The GTST indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

The TCFA flag indicates the status for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA, when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB, when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status for the compare match of GTCCRC.

When GTCCRC performs buffer operation, GTCCRC does not perform compare match.

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status for the compare match of GTCCRD.

When GTCCRD performs buffer operation, GTCCRD does not perform compare match.

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

The TCFE flag indicates the status for the compare match of GTCCRE.

When GTCCRE performs buffer operation, GTCCRE does not perform compare match.

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

The TCFF flag indicates the status for the compare match of GTCCRF.

When GTCCRF performs buffer operation, GTCCRF does not perform compare match.

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR - 1) has occurred
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a trough (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this bit.

ITCNT[2:0] flag (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter)

When the GPTn_OVF/GPTn_UDF interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter is incremented by 1 every time the GPTn_OVF/GPTn_UDF interrupt source which is selected in GTITC.IVTC[1:0] is generated.

These bits are operated independently of the extended interrupt skipping by the GTEITC register.

[Clearing conditions]

- The GPTn_OVF/GPTn_UDF interrupt skipping function is not used (the GTITC.IVTT[2:0] bits are 000b when the IVTC[1:0] bits are 00b).
- The GPTn_OVF/GPTn_UDF interrupt skipping count matches the specified count (the ITCNT[2:0] bits match the skipping count specified by the IVTT[2:0] bits).
- When the count operation is stopped

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and to 0 in down-counting.

ADTRAUF flag (GTADTRA Register Compare Match (Up-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRA register compare match in up-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRA register in up-counting.

[Clearing condition]

- 0 is written to the ADTRAUF flag.

ADTRADF flag (GTADTRA Register Compare Match (Down-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRA register compare match in down-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRA register in down-counting.

[Clearing condition]

- 0 is written to the ADTRADF flag.

ADTRBUF flag (GTADTRB Register Compare Match (Up-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRB register compare match in up-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRB register in up-counting.

[Clearing condition]

- 0 is written to the ADTRBUF flag.

ADTRBDF flag (GTADTRB Register Compare Match (Down-Counting) A/D Conversion Start Request Flag)

This status flag indicates generation of a GTADTRB register compare match in down-counting.

[Setting condition]

- The GTCNT counter matches the GTADTRB register in down-counting.

[Clearing condition]

- 0 is written to the ADTRBDF flag.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits.

When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

DTEF flag (Dead Time Error Flag)

This flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the count period.

This flag returns to 0 when the timer output toggle point after the automatic addition of dead time is back within the period.

This flag can only be read from. (Writing 0 to clear the flag is not allowed.)

When the output disable request by the DTEF flag is enabled (when GTINTAD.GRPDTE bit is 1), the DTEF flag is output as the output disable request to the POEG. The GPT does not have a dead time error interrupt. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- When a change point of the waveform after the automatic setting of dead time has exceeded the count period (in the following cases).
  - Up-counting in triangle-wave mode:
    GTCCRA register – GTDVU register ≤ 0
  - Down-counting in triangle-wave mode:
    GTCCRA register – GTDVD register < 0
  - Up-counting in saw-wave one-shot pulse mode:
    GTCCRA register – GTDVU register < 0, or
    GTCCRA register + GTDVD register > GTPR register
  - Down-counting in saw-wave one-shot pulse mode:
    GTCCRA register + GTDVU register > GTPR register, or
    GTCCRA register - GTDVD register < 0

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the count period.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

When the GTIOCnA or GTIOCnB pin outputs 0, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When the output disable request by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to POEG as an output disable request. The GPT does not have an interrupt to indicate that outputs have been simultaneous driven to the high level. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCnA and GTIOCnB pins output 0 at the same time.

When the GTIOCnA pin or GTIOCnB pin outputs 1, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When the output disable request by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to POEG as an output disable request. The GPT does not have an interrupt to indicate that outputs have been simultaneous driven to the low level. Use the interrupt function in the POEG if this is necessary.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or the OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. Even during the output disable condition, compare match operation continues internally, where the OABHF or OABLF flag is updated based on the operation results.

PCF flag (Period Count Function Finish Flag)

This bit is status flag of period count function finish.

[Setting condition]

- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1 at the end of cycle.
- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 0 at the count clock.

[Clearing condition]

- 0 is written to this bit.

23.2.17 GTBER : General PWM Timer Buffer Enable Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DBRTECB	—	DBRTECA	—	—	—	—	BD3	BD2	BD1	BD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
1	BD1	GTPR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W*1
2	BD2	GTADTRA/GTADTRB Registers Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
3	BD3	GTDVU/GTDVD Registers Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	DBRTECA	GTCCRA Register Double Buffer Repeat Operation Enable 0: GTCCRA register double buffer repeat operation is disabled 1: GTCCRA register double buffer repeat operation is enabled	R/W
9	—	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
10	DBRTECB	GTCCRB Register Double Buffer Repeat Operation Enable 0: GTCCRB register double buffer repeat operation is disabled 1: GTCCRB register double buffer repeat operation is enabled	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
17:16	CCRA[1:0]	GTCCRA Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔GTCCRC) Others: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD)	R/W
19:18	CCRB[1:0]	GTCCRB Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) Others: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	R/W
21:20	PR[1:0]	GTPR Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) Others: Double buffer operation (GTPDBR → GTPBR → GTPR)	R/W
22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	W
23	—	This bit is read as 0. The write value should be 0.	R/W
25:24	ADTTA[1:0]	GTADTRA Register Buffer Transfer Timing Select 0 0: In triangle wave or complementary PWM mode, no transfer. In saw-wave mode, no transfer. 0 1: In triangle wave or complementary PWM mode, transfer at crest. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 0: In triangle wave or complementary PWM mode, transfer at trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 1: In triangle wave or complementary PWM mode, transfer at both crest and trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing.	R/W
26	ADTDA	GTADTRA Register Double Buffer Operation 0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTRA)	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
29:28	ADTTB[1:0]	GTADTRB Register Buffer Transfer Timing Select 0 0: In triangle wave or complementary PWM mode, no transfer. In saw-wave mode, no transfer. 0 1: In triangle wave or complementary PWM mode, transfer at crest. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 0: In triangle wave or complementary PWM mode, transfer at trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing. 1 1: In triangle wave or complementary PWM mode, transfer at both crest and trough. In saw-wave mode, transfer at underflow (in down-counting), overflow (in up-counting), or counter clearing.	R/W
30	ADTDB	GTADTRB Register Double Buffer Operation 0: Single buffer operation (GTADTBRB → GTADTRB) 1: Double buffer operation (GTADTDBRB → GTADTBRB → GTADTRB)	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

The GTBER register provides settings for the buffer operation. Set the GTBER register except the BDx (x = 0 to 3) bits while the GTCNT counter is stopped.

BD0 bit (GTCCR Buffer Operation Disable)

The BD0 bit disables the buffer operation using GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD0 is set to 0, GTCCRB does not perform buffer operation in Saw-wave one-shot pulse mode or Triangle-wave PWM mode. The GTCCRB register is automatically set to a compare match value for negative-phase waveform with dead time.

In complementary PWM mode, it is valid only for the buffer operation of GTCCRC register and GTCCRE register. The buffer operation of GTCCRA registers cannot be disabled. Buffer operation of GTCCRE register and GTCCRF register is enabled/disabled by CP3DB bit of GTBER2 register. No buffer transfer to GTCCRB is performed in complementary PWM mode.

A value for the BD0 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDCE or GTSECR.SBDCD.

When the DBRTECm (m = A, B) bit is 1, setting the BD0 bit to 1 while the mode of operation is saw-wave one-shot pulse mode or triangle-wave PWM mode 3 results in transfer from the intermediate buffer to the GTCCRm register.

BD1 bit (GTPR Buffer Operation Disable)

The BD1 bit disables the buffer operation using GTPR, GTPDBR, and GTPBR combined.

A value for the BD1 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDPE or GTSECR.SBDPD.

In complementary PWM mode, the slave channel is also controlled by setting the BD1 bit of the master channel.

BD2 bit (GTADTRA/GTADTRB Registers Buffer Operation Disable)

This bit disables buffer operation using the GTADTRA, GTADTBRA, and GTADTDBRA registers together and buffer operation using the GTADTRB, GTADTBRB, and GTADTDBRB registers together.

The setting is invalid during the event count operation, and the buffer operation using the GTADTRA and GTADTRB registers is not performed.

A value for the BD2 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the SBDAE or SBDAD bit in the GTSECR register.

BD3 bit (GTDVU/GTDVD Registers Buffer Operation Disable)

In Saw-wave PWM mode 1, Saw-wave one-shot pulse mode or Triangle-wave PWM mode, this bit disables buffer operation using the GTDVU and GTDBU registers together and buffer operation using the GTDVD and GTDBD registers together.

Even though the BD3 bit is set to 0, buffer operation in the GTDVD register is not performed if the GTDTCR.TDFER bit is set to 1. Instead, the value in the GTDVU register is set automatically.

In Saw-wave PWM mode 2 or complementary PWM mode, this bit is invalid and GTDVU and GTDVD registers don’t perform buffer operation.

The setting is invalid during the event count operation, and the buffer operation using the GTDVU and GTDVD registers is not performed.

A value for the BD3 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the SBDDE or SBDDD bit in the GTSECR register.

DBRTECm bits (GTCCRm Register Double Buffer Repeat Operation Enable) (m = A, B)

This setting enables the operation to repeat a transfer to the GTCCRm register from the intermediate buffer by cycle during the buffer transfer disable period when performing the double buffer operation using the GTCCRm register.

It is valid in saw-wave one-shot pulse mode and triangle-wave PWM mode 3.

The disabling period of buffer transfer indicates the period that buffer transfer is stopped by setting of the BD0 bit (CPU writing or simultaneous buffer operation control by the GTSECSR register) and the period for buffer transfer extended skipping (except the case for skipping by counting both crests and troughs) by the GTEITLB register.

When the DBRTECm bit is 1, writing by the CPU to the GTCCRm register sets the same value in temporary register x (x = C, E). The value of the GTCCRx (x = C, E) register is also transferred to the temporary register x (x = C, E) by forcible buffer transfer.

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set the buffer operation with GTCCRA, GTCCRC, and GTCCRD combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough), or complementary PWM mode.

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough), or complementary PWM mode.

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set the buffer operation with GTPR, GTPDBR, and GTPBR combined.

The setting is invalid in complementary PWM mode. Buffer operation unique to complementary PWM mode is performed regardless of the setting value of the PR[1:0] bits.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the 1 is written. This bit is read as 0, and is valid only when counting is stopped with a compare match operation specified.

The setting is invalid in complementary PWM mode.

ADTTA[1:0] bits (GTADTRA Register Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of the GTADTRA, GTADTBRA, and GTADTDBRA registers.

The setting is invalid during the event count operation.

ADTDA bit (GTADTRA Register Double Buffer Operation)

These bits set buffer operation with the GTADTRA, GTADTBRA, and GTADTDBRA registers combined.

The setting is invalid during the event count operation.

ADTTB[1:0] bits (GTADTRB Register Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of the GTADTRB, GTADTBRB, and GTADTDBRB registers.

The setting is invalid during the event count operation.

ADTDB bit (GTADTRB Register Double Buffer Operation)

These bits set buffer operation with the GTADTRB, GTADTBRB, and GTADTDBRB registers combined.

The setting is invalid during the event count operation.

23.2.18 GTITC : General PWM Timer Interrupt and A/D Conversion Start Request Skipping Setting Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ITLA	GTCCRA Register Compare Match/Input Capture Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
1	ITLB	GTCCRB Register Compare Match/Input Capture Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
2	ITLC	GTCCRC Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
3	ITLD	GTCCRD Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
4	ITLE	GTCCRE Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
5	ITLF	GTCCRF Register Compare Match Interrupt Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
7:6	IVTC[1:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select 0 0: Skipping is not performed. 0 1: Both overflow and underflow for saw waves*1 and crest for triangle waves and complementary PWM mode are counted and skipped. 1 0: Both overflow and underflow for saw waves*1 and trough for triangle waves and complementary PWM mode are counted and skipped. 1 1: Both overflow and underflow for saw waves*1 and both crest and trough for triangle waves and complementary PWM mode are counted and skipped.	R/W
10:8	IVTT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select 0 0 0: Skipping is not performed 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
12	ADTAL	GTADTRA Register A/D Conversion Start Request Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
14	ADTBL	GTADTRB Register A/D Conversion Start Request Link 0: Not linked with GPTn_OVF/GPTn_UDF interrupt skipping function. 1: Linked with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
31:15	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Saw-wave PWM mode 2 is not the target of this function.

The GTITC register sets the skipping function for the GTCNT counter overflow (GTPR compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF) and also sets whether to link the other interrupts and A/D conversion start requests with the GPTn_OVF/GPTn_UDF interrupt skipping function. Note the output disable request to POEG cannot be linked with the GPTn_OVF/GPTn_UDF interrupt skipping function. Additionally, if the interrupt skipping function is performed, the change in the status flag is also skipped.

The setting is invalid during the event count operation.

The setting is operated independently of the extended interrupt skipping by the GTEITC register.

ITLA bit (GTCCRA Register Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRA compare match/input capture interrupt (GPTn_CCMPA) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLB bit (GTCCRB Register Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRB compare match/input capture interrupt (GPTn_CCMPB) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLC bit (GTCCRC Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRC compare match interrupt (GPTn_CMPC) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLD bit (GTCCRD Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRD compare match interrupt (GPTn_CMPD) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLE bit (GTCCRE Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRE compare match interrupt (GPTn_CMPE) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLF bit (GTCCRF Register Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRF compare match interrupt (GPTn_CMPF) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

IVTC[1:0] bit (GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select)

These bits set the skipping function for the GTPR compare match (GTCNT counter overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

IVTT[2:0] bit (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select)

These bits set the skipping count for the GTPR compare match (GTCNT counter overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL bit (GTADTRA Register A/D Conversion Start Request Link)

This bit specifies whether to link the GTADTRA A/D conversion start request, which is generated in response to a compare match with the GTCNT counter and the GTADTRA register, with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ADTBL bit (GTADTRB Register A/D Conversion Start Request Link)

This bit specifies whether to link the GTADTRB A/D conversion start request, which is generated in response to a compare match with the GTCNT counter and the GTADTRB register, with the GPTn_OVF/GPTn_UDF interrupt skipping function.

23.2.19 GTCNT : General PWM Timer Counter

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x48

Bit position:	31																														0
Bit field:	GTCNT[31:0]																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	GTCNT[31:0]	GTCNT is a 32-bit read/write counter for GPT32n (n = 0 to 13). GTCNT can only be written to after counting stops. Access in 8-bit or 16-bit units to the GTCNT counter is prohibited, and it should be accessed in 32-bit units. In saw waves or triangle waves, GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.	R/W

23.2.20 GTCCRk : General PWM Timer Compare Capture Register k (k = A to F)

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position:	31																														0
Bit field:	GTCCRk[31:0]																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTCCRk[31:0]	GTCCRk registers are read/write registers. Access in 8-bit or 16-bit units to the GTCCRk register is prohibited, and it should be accessed in 32-bit units. GTCCRA and GTCCRB are registers used for both output compare and input capture. GTCCRC and GTCCRE are compare match registers, and can also function as buffer registers for GTCCRA and GTCCRB. GTCCRD and GTCCRF are compare match registers, and can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).	R/W

23.2.21 GTPR : General PWM Timer Cycle Setting Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x64

Bit position:	31																														0
Bit field:	GTPR[31:0]																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTPR[31:0]	GTPR is a read/write register that sets the maximum count value of GTCNT. Access in 8-bit or 16-bit units to the GTPR register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in the Saw-wave PWM mode 2. For Saw waves except the Saw-wave PWM mode 2, the value of (GTPR + 1) is the cycle. For triangle waves or complementary PWM mode, the value of (GTPR value × 2) is the cycle. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.	R/W

23.2.22 GTPBR : General PWM Timer Cycle Setting Buffer Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x68

Bit position:	31																														0
Bit field:	GTPBR[31:0]																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTPBR[31:0]	GTPBR is a read/write register that functions as a buffer register for GTPR. Access in 8-bit or 16-bit units to the GTPBR register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in Saw-wave PWM mode 2. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.	R/W

23.2.23 GTPDBR : General PWM Timer Cycle Setting Double-Buffer Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x6C

Bit position:	31																														0
Bit field:	GTPDBR[31:0]																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTPDBR[31:0]	The buffer register for the GTPBR register (double buffer register for the GTPR register) Access in 8-bit or 16-bit units to the GTPDBR register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in Saw-wave PWM mode 2. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.	R/W

23.2.24 GTADTRk : A/D Conversion Start Request Timing Register k (k = A, B)

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x70 (GTADTRA)
0x7C (GTADTRB)

Bit position:	31																														0
Bit field:	GTADTRk[31:0]																														
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTADTRk[31:0]	Set the timing of A/D conversion start request generation Access in 8-bit or 16-bit units to the GTADTRk register is prohibited, and it should be accessed in 32-bit units. When the GTADTRk register value matches the GTCNT counter value, an A/D conversion start request is generated. In complementary PWM mode, A/D conversion start request is generated when the GTCNT counter of the master channel matches this register.	R/W

23.2.25 GTADTBRk : A/D Conversion Start Request Timing Buffer Register k (k = A, B)

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x74 (GTADTBRA)
0x80 (GTADTBRB)

Bit position:	31																															0
Bit field:	GTADTBRk[31:0]																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTADTBRk[31:0]	The buffer registers for the GTADTRk register Access in 8-bit or 16-bit units to the GTADTBRk register is prohibited, and it should be accessed in 32-bit units.	R/W

23.2.26 GTADTDBRk : A/D Conversion Start Request Timing Double-Buffer Register k (k = A, B)

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x78 (GTADTDBRA)
0x84 (GTADTDBRB)

Bit position:	31																															0
Bit field:	GTADTDBRk[31:0]																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTADTDBRk[31:0]	The buffer registers for the GTADTBRk register (double buffer registers for the GTADTRk register) Access in 8-bit or 16-bit units to the GTADTDBRk register is prohibited, and it should be accessed in 32-bit units.	R/W

23.2.27 GTDTCR : General PWM Timer Dead Time Control Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDE	Negative-Phase Waveform Setting 0: GTCCRB is set without using GTDVU and GTDVD 1: GTDVU and GTDVD are used to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	TDBUE	GTDVU Register Buffer Operation Enable 0: GTDVU register buffer operation is disabled 1: GTDVU register buffer operation is enabled	R/W
5	TDBDE	GTDVD Register Buffer Operation Enable 0: GTDVD register buffer operation is disabled 1: GTDVD register buffer operation is enabled	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	TDFER	GTDVD Register Setting 0: GTDVU and GTDVD registers are set separately. 1: The value written to GTDVU register is automatically set to GTDVD register.	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. GPT has a dead time control function and GTDVU and GTDVD registers are used for setting dead time value.

This register is invalid in Saw-wave PWM mode 2 or complementary PWM mode.

The setting is invalid during the event count operation.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU and GTDVD. When GTDVU and GTDVD are used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU and GTDVD) is automatically set in GTCCRB.

The TDE bit setting is ignored in saw-wave PWM mode, and the GTCCRB is not automatic setting.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB, and GTST.DTEF flag becomes 1. However, if the obtained GTCCRB value exceeds the upper limit in triangle-wave PWM mode, DTEF flag becomes 0.

- Triangle waves:
  Upper limit value: GTPR − 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode:
  Upper limit value: GTPR
  Lower limit value: 0.

TDBUE bit (GTDVU Register Buffer Operation Enable)

This bit enables buffer operation with the GTDVU and GTDBU registers combined.

The timing of buffer transfer is at troughs in triangle-wave mode, and at overflows or underflows in saw-wave mode.

TDBDE bit (GTDVD Register Buffer Operation Enable)

This bit enables buffer operation with the GTDVD and GTDBD registers combined.

The buffer transfer timing is the trough in triangle-wave mode, and at an overflow or underflow in saw-wave mode.

When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

TDFER bit (GTDVD Register Setting)

This bit sets whether or not the value written to the GTDVU register is also set to the GTDVD register automatically.

23.2.28 GTDVk : General PWM Timer Dead Time Value Register k (k = U, D)

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x8C (GTDVU)
0x90 (GTDVD)

Bit position:	31																															0
Bit field:	GTDVk[31:0]																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTDVk[31:0]	GTDVk is a read/write register that sets the dead time for generating PWM waveforms with dead time. Access in 8-bit or 16-bit units to the GTDVk register is prohibited, and it should be accessed in 32-bit units. The setting is invalid in Saw-wave PWM mode 2. In complementary PWM mode, the GTDVD register is invalid and the GTDVU register is used as the dead time value during both up-counting and down-counting. No matter which GTDVU register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time. In Triangle-waves, The GTDVU register is used for up-counting. The GTDVD register is used for down-counting. In the case of a saw-waves, the GTDVU register controls the front dead time and the GTDVD register controls the rear dead time, regardless of whether the count is up or down. Setting a GTDVk value greater than or equal to GTPR is prohibited. In complementary PWM mode, set the GTDVU register to meet the following conditions: ● GTDVU > 0 ● GTDVU < GTPR/2 ● GTDVU + GTPR ≤ 0xffffffff When using the automatic dead time setting function, do not set a value that makes a change point of the waveform exceeding the count period. The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB register. When GTDVk is used, writing to GTCCRB is prohibited. Other than complementary PWM mode, when this register is set to 0, waveforms without dead time are output. When the GTDTCR.TDFER bit is 1, the writing to the GTDVD register has no effect. At this time, when the GTDVD register is read, the value for the GTDVU register is read. While GPT is running, changing the GTDVk values is prohibited. To change GTDVk to a new value, stop the GPT with the CST bit in the GTCR register.	R/W

23.2.29 GTDBk: General PWM Timer Dead Time Buffer Register k (k = U, D)

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x94 (GTDBU)
0x98 (GTDBD)

Bit position:	31																															0
Bit field:	GTDBk[31:0]																															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	GTDBk[31:0]	The buffer register for the GTDVk register Access in 8-bit or 16-bit units to the GTDBk register is prohibited, and it should be accessed in 32-bit units.	R/W

23.2.30 GTSOS : General PWM Timer Output Protection Function Status Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0x9C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SOS[1:0]	Output Protection Function Status 0 0: Normal operation 0 1: Protected state (GTCCRA = 0 is set during transfer at trough or crest) 1 0: Protected state (GTCCRA ≥ GTPR is set during transfer at trough) 1 1: Protected state (GTCCRA ≥ GTPR is set during transfer at crest)	R
7:2	—	These bits are read as 0.	R
9:8	—	The read value is undefined.	R
31:10	—	These bits are read as 0.	R

The GTSOS register is a status register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (GTDTCR.TDE bit = 1) in triangle-wave mode.

SOS[1:0] bit (Output Protection Function Status)

This bit indicates the status of the output protection function in triangle-wave PWM mode. For details of the output protection function, see section 23.8.4. Output Protection Function for GTIOCnm Pin Output (n = 0 to 13; m = A, B).

23.2.31 GTSOTR : General PWM Timer Output Protection Function Temporary Release Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xA0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOTR	Output Protection Function Temporary Release 0: Protected state is not released 1: Protected state is released	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The GTSOTR register temporarily releases the protected state of GTIOCnB pin output (n = 0 to 13) when output protection has been set.

The protected state can be released only for the case of GTSOS.SOS[1:0] bits are 10b (protected state in which GTCCRA register ≥ GTPR register has occurred during transfer at trough). The protected state cannot be released for any other case.

SOTR bit (Output Protection Function Temporary Release)

This bit sets whether to temporarily release the protected state of the GTIOCnB pin output in an output protected state.

After the SOTR bit has been set to 1, the output protection function is canceled from the first trough. After the SOTR bit has been set to 0, output protection is resumed from the first trough.

23.2.32 GTADSMR : General PWM Timer A/D Conversion Start Request Signal Monitoring Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xA4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	ADSMEN1	—	—	—	—	—	—	ADSMS1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ADSMEN0	—	—	—	—	—	—	ADSMS0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ADSMS0[1:0]	A/D Conversion Start Request Signal Monitor 0 Selection 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting. 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting. 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting. 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	ADSMEN0	A/D Conversion Start Request Signal Monitor 0 Output Enabling 0: Output of A/D conversion start request signal monitor 0 is disabled. 1: Output of A/D conversion start request signal monitor 0 is enabled.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
17:16	ADSMS1[1:0]	A/D Conversion Start Request Signal Monitor 1 Selection 0 0: A/D conversion start request signal generated by the GTADTRA register during up-counting. 0 1: A/D conversion start request signal generated by the GTADTRA register during down-counting. 1 0: A/D conversion start request signal generated by the GTADTRB register during up-counting. 1 1: A/D conversion start request signal generated by the GTADTRB register during down-counting.	R/W
23:18	—	These bits are read as 0. The write value should be 0.	R/W
24	ADSMEN1	A/D Conversion Start Request Signal Monitor 1 Output Enabling 0: Output of A/D conversion start request signal monitor 1 is disabled. 1: Output of A/D conversion start request signal monitor 1 is enabled.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The GTADSMR register is used to control monitors for the A/D conversion start request signal that is synchronized with a frame period.

ADSMSk[1:0] bits (A/D Conversion Start Request Signal Monitor k Selection) (k = 0, 1)

These bits are used to select A/D conversion start request signal synchronized with a frame period which is monitored by the GTASMk pin.

In triangle-wave PWM mode or complementary PWM mode, the following settings are prohibited:

- Set ADSMSk[1:0] bit to 00b (A/D conversion start request during up-counting) when GTADTRA = 0
- Set ADSMSk[1:0] bit to 10b (A/D conversion start request during up-counting) when GTADTRB = 0
- Set ADSMSk[1:0] bit to 01b (A/D conversion start request during down-counting) when GTADTRA = GTPR
- Set ADSMSk[1:0] bit to 11b (A/D conversion start request during down-counting) when GTADTRB = GTPR

ADSMENk bit (A/D Conversion Start Request Signal Monitor k Output Enabling) (k = 0, 1)

This bit enables or disables the monitor output to the GTADSMk pin.

When the output is disabled, the GTADSMk pin goes to the low level.

When the bit is 1, the signal on the GTADSMk pin goes to the high level on assertion of the signal to request to the start of A/D conversion selected by the ADSMSk[1:0] bits and returns to the low level at the end of the current cycle of the timer for the channel that generated the given signal to request the start of A/D conversion. When the counter stops, the value when the counter stopped is retained for output. Set the ADSMENk bit to 0 to output the low level.

When a signal to request the start of A/D conversion is generated at the end of a timer period, the generation of this signal has priority in terms of monitoring output and the output remains at the high level till the end of the next period.

When the output of the same A/D conversion start request signal monitoring output is enabled for multiple channels, ORed signals will be output from the GPT.

23.2.33 GTEITC : General PWM Timer Extended Interrupt Skipping Counter Control Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xA8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EITCNT2[3:0]				EITCNT2IV[3:0]				EIVTT2[3:0]				—	—	EIVTC2[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EITCNT1[3:0]				—	—	—	—	EIVTT1[3:0]				—	—	EIVTC1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	EIVTC1[1:0]	Extended Interrupt Skipping Counter 1 Count Source Select 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in saw-wave mode, and counting crests in triangle-wave mode or complementary PWM mode 1 0: Counting both at overflow or underflow in saw-wave mode, and counting troughs in triangle-wave mode or complementary PWM mode 1 1: Counting both at overflow or underflow in saw-wave mode, and counting both crests and troughs in triangle-wave mode or complementary PWM mode	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	EIVTT1[3:0]	Extended Interrupt Skipping 1 Skipping Count Setting Skipping count for the extended interrupt skipping 1	R/W
11:8	—	These bits are read as 0. The write value should be 0.	R/W
15:12	EITCNT1[3:0]	Extended Interrupt Skipping Counter 1	R
17:16	EIVTC2[1:0]	Extended Interrupt Skipping Counter 2 Count Source select 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in saw-wave mode, and counting crests in triangle-wave mode or complementary PWM mode 1 0: Counting both at overflow or underflow in saw-wave mode, and counting troughs in triangle-wave mode or complementary PWM mode 1 1: Counting both at overflow or underflow in saw-wave mode, and counting both crests and troughs in triangle-wave mode or complementary PWM mode	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R/W
23:20	EIVTT2[3:0]	Extended Interrupt Skipping 2 Skipping Count Setting Skipping count for the extended interrupt skipping 2	R/W
27:24	EITCNT2IV[3:0]	Extended Interrupt Skipping Counter 2 Initial Value	R/W*1
31:28	EITCNT2[3:0]	Extended Interrupt Skipping Counter 2	R

Note 1. The EITCNT2IV[3:0] bits are only writable when the value other than 00b is written to the EIVTC2[1:0] bits that have been 00b.

GTEITC register sets the extended interrupt skipping function to skip the interrupts, A/D conversion start requests, and buffer transfers independently by counting at overflow and underflow in the GTCNT counter.

The setting is operated independently of the interrupt skipping by the GTITC register or the GTADCMSC register.

The setting is invalid during the event count operation.

Access in 8-bit units to GTEITC is prohibited.

EIVTCk[1:0] bits (Extended Interrupt Skipping Counter k Count Source Select) (k = 1, 2)

These bits select the way of counting for the extended interrupt skipping counter k.

Setting only with these bits does not skip the interrupts, A/D conversion start requests, and buffer transfers. Skipping function for the interrupt, A/D conversion start request, and buffer transfer, all of which are a target of skipping, is set individually with the GTEITLI1, GTEITLI2, and GTEITLB registers.

EIVTTk[3:0] bits (Extended Interrupt Skipping k Skipping Count Setting) (k = 1, 2)

A count for the period with continuous skipping is set as a skipping count, where a period is from a generation of a count source selected by the EIVTCk[1:0] bits to the next generation of the count source.

When the count source is generated while the EIVTTk[3:0] bits match the EITCNTk[3:0] bits, the EITCNTk[3:0] bits are cleared.

When these bits are 0x0, skipping is not performed.

EITCNT1[3:0] bits (Extended Interrupt Skipping Counter 1)

The counting is incremented by 1 every time a count source (overflow/underflow/crest/trough) selected by the EIVTC1[1:0] bits is generated.

Counting is performed periodically within the range between 0 and the EIVTT1[3:0] bits.

Even if the GTCNT counter is stopped, the value is not cleared, and value at stop of the GTCNT counter is retained.

[Clearing conditions]

- 00b is written to the EIVTC1[1:0] bits.
- 0x0 is written to the EIVTT1[3:0] bits.
- A count source (overflow/underflow/crest/trough) selected by the EIVTC1[1:0] bits is generated when the extended interrupt skipping 1 skipping count set by the EIVTT1[3:0] bits match the value for the EITCNT1[3:0]

EITCNT2IV[3:0] bit (Extended Interrupt Skipping Counter 2 Initial Value)

These bits are the value of the initial value for the extended interrupt skipping counter 2.

Writing to the EITCNT2IV[3:0] is performed only when the writing value to the EIVTC2[1:0] bits are other than 00b and when the GTEITC register is written by the access of upper 16 bits or 32 bits while the EITCNT2[3:0] bits are set not to count (EIVTC2[1:0] bits are 00b). When the EITCNT2IV[3:0] bits are written, the value written to the EITCNT2IV[3:0] bits is written to the EITCNT2[3:0] bits simultaneously.

The writing to the EITCNT2IV[3:0] bits are ignored when the EITCNT2[3:0] bits are set to count (EIVTC2[1:0] bits are other than 00b) or perform the setting of not to count (00b is written to the EIVTC2[1:0] bits).

The EITCNT2IV[3:0] bits are not reset by the writing 00b to the EIVTC2[1:0] bits.

EITCNT2[3:0] bit (Extended Interrupt Skipping Counter 2)

The counting is incremented by 1 every time a count source (overflow/underflow/crest/trough) selected by the EIVTC2[1:0] bits is generated.

Counting is performed periodically within the range between 0 and the EIVTT2[3:0] bits.

Even if the GTCNT counter is stopped, the value is not cleared, and value at stop of the GTCNT counter is retained.

Setting of the initial value for the EITCNT2[3:0] bits are performed only when the writing value to the EIVTC2[1:0] bits are other than 00b and when the GTEITC register is written by the access of upper 16 bits or 32 bits while the extended interrupt skipping counter 2 is set as not to count (EIVTC2[1:0] bits are 00b).

When the initial value is set, the written value to the EITCNT2IV[3:0] bits is written to the EITCNT2[3:0] bits as the initial value.

[Clearing condition]

- 00b is written to the EIVTC2[1:0] bits.
- 0x0 is written to the EIVTT2[3:0] bits.
- The value other than 00b is written to the EIVTC2[1:0] bits and the 0x0 is written to the EITCNT2IV[3:0] bits simultaneously while 00b is set to the EIVTC2[1:0] bits.
- A count source (overflow/underflow/crest/trough) selected by the EIVTC2[1:0] bits is generated when the extended interrupt skipping 2 skipping count set by the EIVTT2[3:0] bits match the value for the EITCNT2[3:0].

23.2.34 GTEITLI1 : General PWM Timer Extended Interrupt Skipping Setting Register 1

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xAC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	EITLU[2:0]			—	EITLV[2:0]			—	EITLF[2:0]			—	EITLE[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	EITLD[2:0]			—	EITLC[2:0]			—	EITLB[2:0]			—	EITLA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EITLA[2:0]	GTCCRA Register Compare Match/Input Capture Interrupt Extended Skipping Function Select See Table 23.6.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	EITLB[2:0]	GTCCRB Register Compare Match/Input Capture Interrupt Extended Skipping Function Select See Table 23.6.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	EITLC[2:0]	GTCCRC Register Compare Match Interrupt Extended Skipping Function Select See Table 23.6.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
14:12	EITLD[2:0]	GTCCRD Register Compare Match Interrupt Extended Skipping Function Select See Table 23.6.	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
18:16	EITLE[2:0]	GTCCRE Register Compare Match Interrupt Extended Skipping Function Select See Table 23.6.	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
22:20	EITLF[2:0]	GTCCRF Register Compare Match Interrupt Extended Skipping Function Select See Table 23.6.	R/W
23	—	This bit is read as 0. The write value should be 0.	R/W
26:24	EITLV[2:0]	Overflow Interrupt Extended Skipping Function Select See Table 23.6.	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	EITLU[2:0]	Underflow Interrupt Extended Skipping Function Select See Table 23.6.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The GTEITLI1 register sets the extended skipping function for interrupts such as compare match/input capture, overflow and underflow.

Setting only with this register does not perform skipping. The GTEITC register should be set so that a corresponding extended interrupt skipping counter operates the counting.

The setting is operated independently of the interrupt skipping by the GTITC register or the GTADCMSC register.

The setting is invalid during the event count operation.

EITLm[2:0] bits (GTCCRm Register Compare Match/Input Capture Interrupt Extended Skipping Function Select) (m = A, B)

These bits select the extended interrupt skipping function to skip the compare match/input capture interrupt (GPTn_CCMPm) in the GTCCRm register. See Table 23.6.

EITLx[2:0] bits (GTCCRx Register Compare Match Interrupt Extended Skipping Function Select) (x = C, D, E, F)

These bits select the extended interrupt skipping function to skip the compare match interrupt (GPTn_CMPx) in the GTCCRx register. See Table 23.6.

EITLV[2:0] bit (Overflow Interrupt Extended Skipping Function Select)

These bits select the extended interrupt skipping function to skip the interrupt at overflow(GPTn_OVF). See Table 23.6.

EITLU[2:0] bit (Underflow Interrupt Extended Skipping Function Select)

These bits select the extended interrupt skipping function to skip the interrupt at underflow (GPTn_UDF). See Table 23.6.

Table 23.6 Setting the Function select for the GTEITLI1

EITLy[2:0]	Function
0 0 0	Do not perform an extended interrupt skipping
0 0 1	Skip an interrupt in the period when the value for the extended interrupt skipping counter 1 is other than 0 (An interrupt is output in the period of the EITCNT1[3:0] bits = 0)
0 1 0	Skip an interrupt in the period when the value for the extended interrupt skipping counter 2 is other than 0 (An interrupt is output in the period of the EITCNT2[3:0] bits = 0)
0 1 1	Skip an interrupt in the period the value for the extended interrupt skipping counter 1 or 2 is other than 0 (An interrupt is output in the period of the EITCNT1[3:0] bits = 0 and the EITCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip an interrupt in the period when the value for the extended interrupt skipping counter 1 is other than the skipping count (An interrupt is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits)
1 1 0	Skip an interrupt in the period when the value for the extended interrupt skipping counter 2 is other than the skipping count (An interrupt is output in the period of the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)
1 1 1	Skip an interrupt in the period when the value for the extended interrupt skipping counter 1 or 2 is other than the skipping count (An interrupt is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits and the EITCNT2 [3:0] bits = the EIVTT2[3:0] bits)

Note:
- y = A, B, C, D, E, F, V, U
- When the intended skipping counter is set as not to count (the EIVTCk[1:0] bits = 00b or the EIVTTk[3:0] bits = 0x0), skipping is not performed.(k = 1, 2)
- When the EITLy[2:0] bits are set to 011b or 111b, and when one of the skipping counter 1 or 2 is set as not to count, skipping is not performed.

23.2.35 GTEITLI2 : General PWM Timer Extended Interrupt Skipping Setting Register 2

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xB0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	EADTBL[2:0]			—	EADTAL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EADTAL[2:0]	GTADTRA Register A/D Conversion Start Request Extended Skipping Function Select See Table 23.7.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	EADTBL[2:0]	GTADTRB Register A/D Conversion Start Request Extended Skipping Function Select See Table 23.7.	R/W
31:7	—	These bits are read as 0. The write value should be 0.	R/W

The GTEITLI2 register sets the extended skipping function for A/D conversion start requests.

Setting only with this register does not perform skipping. The GTEITC register should be set so that a corresponding extended interrupt skipping counter operates the counting.

The setting is operated independently of the interrupt skipping by the GTITC register or the GTADCMSC register.

The setting is invalid during the event count operation.

EADTmL[2:0] bits (GTADTRm Register A/D Conversion Start Request Extended Skipping Function Select) (m = A, B)

These bits select the extended skipping function to skip A/D conversion start requests for the compare match in the GTADTRm register. See Table 23.7.

Table 23.7 Setting the Function Select for the GTEITLI2 Register

EADTmL[2:0]	Function
0 0 0	Do not perform an extended interrupt skipping
0 0 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 is other than 0 (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = 0)
0 1 0	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 2 is other than 0 (An A/D conversion start request is output in the period of the EITCNT2[3:0] bits = 0)
0 1 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 or 2 is other than 0 (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = 0 and the EITCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 is other than the skipping count (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits)
1 1 0	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 2 is other than the skipping count (An A/D conversion start request is output in the period of the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)
1 1 1	Skip an A/D conversion start request in the period when the value for the extended interrupt skipping counter 1 or 2 is other than the skipping count (An A/D conversion start request is output in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits and the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)

Note:
- m = A, B
- When the intended skipping counter is set as not to count (the EIVTCk[1:0] bits = 00b or the EIVTTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the EADTmL[2:0] bits are set to 011b or 111b, and when one of the skipping counter 1 or 2 is set as not to count, skipping is not performed.

23.2.36 GTEITLB : General PWM Timer Extended Buffer Transfer Skipping Setting Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xB4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	EBTLDVD[2:0]			—	EBTLDVU[2:0]			—	EBTLADB[2:0]			—	EBTLADA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EBTLPR[2:0]			—	EBTLCB[2:0]			—	EBTLCA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EBTLCA[2:0]	GTCCRA Register Buffer Transfer Extended Skipping Function Select See Table 23.8.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	EBTLCB[2:0]	GTCCRB Register Buffer Transfer Extended Skipping Function Select See Table 23.8.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	EBTLPR[2:0]	GTPR Register Buffer Transfer Extended Skipping Function Select See Table 23.8.	R/W*1
15:11	—	These bits are read as 0. The write value should be 0.	R/W
18:16	EBTLADA[2:0]	GTADTRA Register Buffer Transfer Extended Skipping Function Select See Table 23.8.	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
22:20	EBTLADB[2:0]	GTADTRB Register Buffer Transfer Extended Skipping Function Select See Table 23.8.	R/W
23	—	This bit is read as 0. The write value should be 0.	R/W
26:24	EBTLDVU[2:0]	GTDVU Register Buffer Transfer Extended Skipping Function Select See Table 23.8.	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	EBTLDVD[2:0]	GTDVD Register Buffer Transfer Extended Skipping Function Select See Table 23.8.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.

The GTEITLB register sets the extended skipping function for buffer transfers.

Setting only this register does not perform skipping. The GTEITC register should be set so that a corresponding extended interrupt skipping counter operates the counting.

The setting is operated independently of the interrupt skipping by the GTITC register.

The buffer transfer from the GTOLBR register to the GTIOR.GTIOA[4:0], GTIOB[4:0] bits is not target of the extended buffer transfer skipping function.

The setting is invalid during the event count operation.

EBTLCA[2:0] bit (GTCCRA Register Buffer Transfer Extended Skipping Function Select)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTCCRA, GTCCRC, GTCCRD registers and a temporary register A) in the GTCCRA register. See Table 23.8.

An extended skipping of buffer transfers in the GTCCRA register is valid for forcible buffer transfers by the GTBER.CCRSWT bit while the count operation is stopped. Forcible buffer transfers in the GTCCRA register should be performed in the condition of not performing the extended buffer transfer skipping.

The buffer transfer between the GTCCRC, GTCCRE, and GTCCRA in complementary PWM mode cannot be skipped.

EBTLCB[2:0] bit (GTCCRB Register Buffer Transfer Extended Skipping Function Select)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTCCRB, GTCCRE, GTCCRF registers and a temporary register B) in the GTCCRB register. See Table 23.8.

An extended skipping of buffer transfers in the GTCCRB register is valid for forcible buffer transfers by the GTBER.CCRSWT bit while the count operation is stopped. Forcible buffer transfers in the GTCCRB register should be performed in the condition of not performing the extended buffer transfer skipping.

EBTLPR[2:0] bit (GTPR Register Buffer Transfer Extended Skipping Function Select)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTPR, GTPBR, and GTPDBR registers) in the GTPR register. See Table 23.8.

If the buffer transfer of GTPR is skipped in complementary PWM mode, GTEITC setting of slave channel should be matched to the master channel so that the buffer transfer timing of the slave channel matches the master channel.

EBTLADm[2:0] bits (GTADTRm Register Buffer Transfer Extended Skipping Function Select) (m = A, B)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers among the GTADTRm, GTADTBRm, and GTADTDBRm registers) in the GTADTRm register. See Table 23.8.

EBTLDVm[2:0] bits (GTDVm Register Buffer Transfer Extended Skipping Function Select) (m = U, D)

These bits select the extended buffer transfer skipping function to skip buffer transfers (transfers between the GTDVm and GTDBm registers) in the GTDVm register. See Table 23.8.

Table 23.8 Setting the Function Select for the GTEITLB Register

EBTLx[2:0] bits	Function
0 0 0	Do not perform an extended interrupt skipping
0 0 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 is other than 0 (Buffer is transferred in the period of the EITCNT1[3:0] bits = 0)
0 1 0	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 2 is other than 0 (Buffer is transferred in the period of the EITCNT2[3:0] bits = 0)
0 1 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 or 2 is other than 0 (Buffer is transferred in the period of the EITCNT1[3:0] bits = 0 and the EITCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 is other than the skipping count (Buffer is transferred in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits)
1 1 0	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 2 is other than the skipping count (Buffer is transferred in the period of the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)
1 1 1	Skip a buffer transfer in the period when the value for the extended interrupt skipping counter 1 or 2 is other than the skipping count (Buffer is transferred in the period of the EITCNT1[3:0] bits = the EIVTT1[3:0] bits and the EITCNT2[3:0] bits = the EIVTT2[3:0] bits)

Note:
- x = CA, CB, PR, ADA, ADB, DVU, DVD
- When the intended skipping counter is set as not to count (EIVTCk[1:0]bits = 00b or EIVTTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the EBTLx[2:0] bits are set to 011b or 111b, and when one of the skipping counter 1 or 2 is set as not to count, skipping is not performed.

23.2.37 GTICLF : General PWM Timer Inter Channel Logical Operation Function Setting Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xB8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	ICLFSELD[5:0]						—	ICLFB[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ICLFSELC[5:0]						—	ICLFA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ICLFA[2:0]	GTIOCnA Output Logical Operation Function Select 0 0 0: A (no delay) 0 0 1: NOT A (no delay) 0 1 0: C (1GTCLK delay) 0 1 1: NOT C (1GTCLK delay) 1 0 0: A AND C (1GTCLK delay)*2 1 0 1: A OR C (1GTCLK delay)*2 1 1 0: A EXOR C (1GTCLK delay)*2 1 1 1: A NOR C (1GTCLK delay)*2	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
9:4	ICLFSELC[5:0]	Inter Channel Signal C Select*1*2 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B ⋮ 0x12: GTIOC9A 0x13: GTIOC9B Others: Setting prohibited	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
18:16	ICLFB[2:0]	GTIOCnB Output Logical Operation Function Select 0 0 0: B (no delay) 0 0 1: NOT B (no delay) 0 1 0: D (1GTCLK delay) 0 1 1: NOT D (1GTCLK delay) 1 0 0: B AND D (1GTCLK delay)*3 1 0 1: B OR D (1GTCLK delay)*3 1 1 0: B EXOR D (1GTCLK delay)*3 1 1 1: B NOR D (1GTCLK delay)*3	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
25:20	ICLFSELD[5:0]	Inter Channel Signal D Select*1*3 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B ⋮ ⋮ 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The signal before performing output disable control is selected.
Note 2. When channel's own GTIOCnA is selected, C is treated as "1".
Note 3. When channel's own GTIOCnB is selected, D is treated as "1".

The GTICLF register sets the logical operation function between compare match outputs. The logical operation is performed with the signals that the duty 0%/100% control is performed after compare match control. (The output disable control is performed with the signal after logical operation.)

Access in 8-bit units to GTICLF is prohibited.

ICLFm[2:0] bit (GTIOCnm Output Logical Operation Function Select) (m = A, B)

These bits select the logical operation function between signals before performing output disable control for GTIOCnm. To prevent hazard to the GPT output, the signal after logical operation is latched with GTCLK. After latching, the output disable control is performed. When the logical operation function which causes the delay of 1 GTCLK is selected, the output enable signal is also delayed with 1 GTCLK and input to the output disable control.

When the same signal to operate logical function AND, OR, EXOR and NOR is selected, one signal is treated as "1".

ICLFSELk[5:0] bit (Inter Channel Signal k Select) (k = C, D)

These bits select the signal k that the logical operation is performed with the signal before performing output disable control for GTIOCnm.

23.2.38 GTPC : General PWM Timer Period Count Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 3, 10 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xBC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PCNT[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ASTP	—	—	—	—	—	—	—	PCEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PCEN	Period Count Function Enable 0: Period count function is disabled 1: Period count function is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
8	ASTP	Automatic Stop Function Enable 0: Automatic stop function is disabled 1: Automatic stop function is enabled	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
27:16	PCNT[11:0]	Period Counter Counter for the number of period	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTPC register counts the number of period.

PCEN bit (Period Count Function Enable)

This bit enables or disables period count function.

Writing is available when counting is both in progress and stopped.

When 1 is written to either the GTSECR.SPCE bit or the GTSECR.SPCD bit, the value is simultaneously set to the PCEN bit in the channels set to 1 by the GTSECSR register.

ASTP bit (Automatic Stop Function Enable)

This bit enables or disables the GTCNT counter automatic stopping after finishing counting the number of period.

When the PCEN bis is 0, writing is available.

When the PCEN bit is 1, writing is disabled.

When the PCEN bit is 1, the ASTP bit is 1, and the PCNT counter is stopped at PCNT = 0, the GTCNT counter is also stopped. When the ASTP bit is 0, the GTCNT counter continues to count.

PCNT[11:0] bit (Period Counter)

This counter counts the number of period.

When the PCEN bis is 0, writing the number of period is available.

When the PCEN bit is 1, writing is disabled, and down-counting is performed at the end of period. In saw-wave mode, the end of period refers to overflow, underflow, or counter clearing. In triangle-wave mode or complementary PWM mode, it refers to trough.

When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immediately after that.

23.2.39 GTADCMSC : General PWM Timer A/D Conversion Start Request Compare Match Skipping Control Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xC0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ADCMSCNT2[3:0]				ADCMSCNT2IV[3:0]				ADCMST2[3:0]				—	—	ADCMSC2[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADCMSCNT1[3:0]				ADCMSCNT1IV[3:0]				ADCMST1[3:0]				—	—	ADCMSC1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ADCMSC1[1:0]	A/D Conversion Start Request Compare Match Skipping Counter 1 Count Source Select 0 0: Not counted (not skipped) 0 1: Counting GTADTRA register compare match 1 0: Counting GTADTRB register compare match 1 1: Counting both GTADTRA register compare match and GTADTRB register compare match	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	ADCMST1[3:0]	A/D Conversion Start Request Compare Match Skipping 1 Skipping Count Setting Skipping count for the A/D conversion start request compare match skipping 1.	R/W
11:8	ADCMSCNT1IV[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 1 Initial Value	R/W*1
15:12	ADCMSCNT1[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 1	R
17:16	ADCMSC2[1:0]	A/D Conversion Start Request Compare Match Skipping Counter 2 Count Source Select 0 0: Not counted (not skipped) 0 1: Counting GTADTRA register compare match 1 0: Counting GTADTRB register compare match 1 1: Counting both GTADTRA register compare match and GTADTRB register compare match	R/W
19:18	—	These bits are read as 0. The write value should be 0.	R/W
23:20	ADCMST2[3:0]	A/D Conversion Start Request Compare Match Skipping 2 Skipping Count Setting Skipping count for the A/D conversion start request compare match skipping 2	R/W
27:24	ADCMSCNT2IV[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 2 Initial Value	R/W*2
31:28	ADCMSCNT2[3:0]	A/D Conversion Start Request Compare Match Skipping Counter 2	R

Note 1. Writing is possible only when the ADCMSC1[1:0] bits are 00b and a value other than 00b is written to the ADCMSC1[1:0] bits.
Note 2. Writing is possible only when the ADCMSC2[1:0] bits are 00b and a value other than 00b is written to the ADCMSC2[1:0] bits.

The GTADCMSC register is a register that controls the skipping counter of the A/D conversion start request compare match skipping function that counts compare matches of GTADTRA register and GTADTRB register, and skipping A/D conversion start request and buffer transfer independently.

This register setting is operated independently of the interrupt skipping by the GTITC register or GTEITC register.

Access in 8-bit units to GTADCMSC is prohibited.

ADCMSCk[1:0] bits (A/D Conversion Start Request Compare Match Skipping Counter k Count Source Select) (k = 1, 2)

These bits select the way of counting for the A/D conversion start request compare match skipping counter k.

Setting only with these bits does not skip the A/D conversion start requests and buffer transfers. Skipping function for the A/D conversion start request and buffer transfer which are a target of skipping is set individually with the GTADCMSS register.

ADCMSTk[3:0] bits (A/D Conversion Start Request Compare Match Skipping k Skipping Count Setting) (k = 1, 2)

A count for the period with continuous skipping is set as a skipping count, where a period is from a generation of a count source selected by the ADCMSCk[1:0] bits to the next generation of the count source.

When the count source is generated while the ADCMSTk[3:0] bits match the ADCMSCNTk[3:0] bits, the ADCMSCNTk[3:0] bits are cleared.

When these bits are 0x0, skipping is not performed.

ADCMSCNTkIV[3:0] bits (A/D Conversion Start Request Compare Match Skipping Counter k Initial Value) (k = 1, 2)

These bits are the value of the initial value for the A/D conversion start request compare match skipping counter k.

Writing to the ADCMSCNTkIV[3:0] is performed only when the writing value to the ADCMSCk[1:0] bits are other than 00b and when the GTADCMSC register is written by the access of 16 bits or 32 bits while the ADCMSCNTk[3:0] bits are set not to count (ADCMSCk[1:0] bits are 00b). When the ADCMSCNTkIV[3:0] bits are written, the value written to the ADCMSCNTkIV[3:0] bits is written to the ADCMSCNTk[3:0] bits simultaneously.

The writing to the ADCMSCNTkIV[3:0] bits are ignored when the ADCMSCNTk[3:0] bits are set to count (ADCMSCk[1:0] bits are other than 00b) or perform the setting of not to count (00b is written to the ADCMSCk[1:0] bits).

The ADCMSCNTkIV[3:0] bits are not reset by the writing 00b to the ADCMSCk[1:0] bits.

ADCMSCNTk[3:0] bits (A/D Conversion Start Request Compare Match Skipping Counter k) (k=1,2)

The counting is incremented by 1 every time a count source selected by the ADCMSCk[1:0] bits is generated.

Counting is performed periodically within the range between 0 and the ADCMSTk[3:0] bits.

Even if the GTCNT counter is stopped, the value is not cleared, and value at stop of the GTCNT counter is retained.

Setting of the initial value for the ADCMSCNTk[3:0] bits are performed only when the writing value to the ADCMSCk[1:0] bits are other than 00b and when the GTADCMSC register is written by the access of 16 bits or 32 bits while the A/D conversion start request compare match skipping counter k is set as not to count (ADCMSCk[1:0] bits are 00b).

When the initial value is set, the written value to the ADCMSCNTkIV[3:0] bits is written to the ADCMSCNTk[3:0] bits as the initial value.

[Clearing condition]

- 00b is written to the ADCMSCk[1:0] bits.
- 0x0 is written to the ADCMSTk[3:0] bits.
- The value other than 00b is written to the ADCMSCk[1:0] bits and the 0x0 is written to the ADCMSCNTkIV[3:0] bits simultaneously while 00b is set to the ADCMSCk[1:0] bits.
- A count source selected by the ADCMSCk[1:0] bits is generated when the extended interrupt skipping 2 skipping count set by the ADCMSTk[3:0] bits match the value for the ADCMSCNTk[3:0].

23.2.40 GTADCMSS : General PWM Timer A/D Conversion Start Request Compare Match Skipping Setting Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xC4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	ADCMBSB[2:0]			—	ADCMBSA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	ADCMSBL[2:0]			—	ADCMSAL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADCMSAL[2:0]	GTADTRA Register A/D Conversion Start Request Compare Match Skipping Function Select See Table 23.9.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	ADCMSBL[2:0]	GTADTRB Register A/D Conversion Start Request Compare Match Skipping Function Select See Table 23.9.	R/W
15:7	—	These bits are read as 0. The write value should be 0.	R/W
18:16	ADCMBSA[2:0]	GTADTRA Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select See Table 23.10.	R/W

Bit	Symbol	Function	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
22:20	ADCMBSB[2:0]	GTADTRB Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select See Table 23.10.	R/W
31:23	—	These bits are read as 0. The write value should be 0.	R/W

The GTADCMSS register is a register that selects the A/D conversion start request compare match skipping function or the GTADTRm (m = A, B) register buffer transfer by A/D conversion start request compare match skipping function.

Setting only with this register does not perform skipping. The GTADCMSC register should be set so that a corresponding A/D conversion start request compare match skipping counter operates the counting.

This register setting is operated independently of the interrupt skipping by the GTITC register or GTEITC register.

ADCMSmL[2:0] bits (GTADTRm Register A/D Conversion Start Request Compare Match Skipping Function Select) (m = A, B)

These bits select the A/D conversion start request compare match skipping function of the GTADTRm (m = A, B) register.Table 23.9.

ADCMBSm[2:0] bits (GTADTRm Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select) (m = A, B)

These bits select the GTADTRm (m = A, B) register buffer transfer by A/D conversion start request compare match skipping function which skips the buffer transfer of GTADTRm (m = A, B) register (Transfer between GTADTRm register, GTADTBRm register, GTADTDBRm register). See Table 23.10.

Table 23.9 Setting of the GTADTRm Register A/D Conversion Start Request Compare Match Skipping Function Select bit (m = A, B)

ADCMSmL[2:0]	Function
0 0 0	Do not perform an A/D conversion start request compare match skipping
0 0 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than 0 (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = 0)
0 1 0	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than 0 (An A/D conversion start request is output in the period of the ADCMSCNT2[3:0] bits = 0)
0 1 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than 0 (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = 0 and the ADCMSCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than the skipping count (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits)
1 1 0	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than the skipping count (An A/D conversion start request is output in the period of the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)
1 1 1	Skip an A/D conversion start request in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than the skipping count (An A/D conversion start request is output in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits and the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)

Note:
- m = A, B
- When the intended skipping counter is set as not to count (the ADCMSCk[1:0] bits = 00b or the ADCMSTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the ADCMSmL[2:0] bits are set to 011b or 111b, and when one of the skipping counters is set as not to count, skipping is not performed.

Table 23.10 Setting of the GTADTRm Register Buffer Transfer by A/D Conversion Start Request Compare Match Skipping Function Select bit (m = A, B)

ADCMBSm[2:0]	Function
0 0 0	Do not perform an GTADTRm register buffer transfer by A/D conversion start request compare match skipping
0 0 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than 0 (Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = 0)
0 1 0	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than 0 (Buffer is transferred in the period of the ADCMSCNT2[3:0] bits = 0)
0 1 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than 0 (Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = 0 and the ADCMSCNT2[3:0] bits = 0)
1 0 0	Setting prohibited
1 0 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 is other than the skipping count (Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits)
1 1 0	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 2 is other than the skipping count (Buffer is transferred in the period of the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)
1 1 1	Skip a buffer transfer in the period when the value for the A/D conversion start request compare match skipping counter 1 or 2 is other than the skipping count (A Buffer is transferred in the period of the ADCMSCNT1[3:0] bits = the ADCMST1[3:0] bits and the ADCMSCNT2[3:0] bits = the ADCMST2[3:0] bits)

Note:
- m = A, B
- When the intended skipping counter is set as not to count (the ADCMSCk[1:0] bits = 00b or the ADCMSTk[3:0] bits = 0x0), skipping is not performed. (k = 1, 2)
- When the ADCMSmL[2:0] bits are set to 011b or 111b, and when one of the skipping counters is set as not to count, skipping is not performed.

23.2.41 GTSECSR : General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xD0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	SECSEL13	SECSEL12	SECSEL11	SECSEL10	SECSEL9	SECSEL8	SECSEL7	SECSEL6	SECSEL5	SECSEL4	SECSEL3	SECSEL2	SECSEL1	SECSEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SECSEL0	Channel 0 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
1	SECSEL1	Channel 1 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
2	SECSEL2	Channel 2 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W

Bit	Symbol	Function	R/W
3	SECSEL3	Channel 3 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
4	SECSEL4	Channel 4 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
5	SECSEL5	Channel 5 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
6	SECSEL6	Channel 6 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
7	SECSEL7	Channel 7 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
8	SECSEL8	Channel 8 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
9	SECSEL9	Channel 9 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
10	SECSEL10	Channel 10 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
11	SECSEL11	Channel 11 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
12	SECSEL12	Channel 12 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
13	SECSEL13	Channel 13 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
31:14	—	These bits are read as 0. The write value should be 0.	R/W

The GTSECSR register selects an intended channel n (n = 0 to 13) for updating an operation enable bit by the GTSECR register. A bit position for the GTSECSR register indicates a channel number. The GTSECSR register of each channel is a common register, and writing 1 to a bit in the GTSECSR register in any channel and updating it changes a channel, related to the position of the bit written with 1 by the GTSECSR register, to be simultaneously controlled of the operation enable bit by the GTSECR register.

Contrary to a security attribute for write or read access, if the security and privilege attributes set on each channel has the security violation or the privilege violation, the bit of the channel number that violates security cannot be written or read, and the read value of the bit is 0.

Access in 8-bit or 16-bit units to GTSECSR is prohibited, and it should be accessed in 32-bit units.

SECSELn bit (Operation Enable Bit Simultaneous Control Channel Select) (n = 0 to 13)

This bit enables or disables the simultaneous control of operation enable in channel n.

When the bit is set to 1, the simultaneous control is enabled, and disabled when the bit is 0.

23.2.42 GTSECR : General PWM Timer Operation Enable Bit Simultaneous Control Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xD4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	SSCD	SPCD	—	—	—	—	—	—	SSCE	SPCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SBDDD	SBDAD	SBDPD	SBDCD	—	—	—	—	SBDDE	SBDAE	SBDPE	SBDCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SBDCE	GTCCR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTCCR buffer operations 1: Enable GTCCR register buffer operations simultaneously	R/W
1	SBDPE	GTPR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTPR buffer operations 1: Enable GTPR register buffer operations simultaneously	R/W*1
2	SBDAE	GTADTR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTADTR buffer operations 1: Enable GTADTR register buffer operations simultaneously	R/W
3	SBDDE	GTDV Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTDV buffer operations 1: Enable GTDV register buffer operations simultaneously	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	SBDCD	GTCCR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTCCR buffer operations 1: Disable GTCCR register buffer operations simultaneously	R/W
9	SBDPD	GTPR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTPR buffer operations 1: Disable GTPR register buffer operations simultaneously	R/W*1
10	SBDAD	GTADTR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTADTR buffer operations 1: Disable GTADTR register buffer operations simultaneously	R/W
11	SBDDD	GTDV Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTDV buffer operations 1: Disable GTDV register buffer operations simultaneously	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	SPCE	Period Count Function Simultaneous Enable*2 0: Disable simultaneous enabling period count function 1: Enable period count function simultaneously	R/W
17	SSCE	Synchronous Set/Clear Simultaneous Enable*3 0: Disable simultaneous enabling synchronous set/clear 1: Enable synchronous set/clear simultaneously	R/W*1
23:18	—	These bits are read as 0. The write value should be 0.	R/W
24	SPCD	Period Count Function Simultaneous Disable*2 0: Disable simultaneous disabling period count function 1: Disable period count function simultaneously	R/W

Bit	Symbol	Function	R/W
25	SSCD	Synchronous Set/Clear Simultaneous Disable*3 0: Disable simultaneous disabling synchronous set/clear 1: Disable synchronous set/clear simultaneously	R/W*1
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.
Note 2. This bit is only available in GPT320 to GPT323 and GPT3210 to GPT3213.
In GPT324 to GPT329, this bit is read as 0. The write value should be 0.
Note 3. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.

The GTSECR register simultaneously updates the value for operation enable bits of a channel set by the GTSECSR register.

Writing 1 to a bit in the GTSECR register in any channel and updating it updates an operation enable bit for all channels, related to the position of the bit written with 1 by the all GTSECSR registers.

Contrary to a security attribute for write or read access, if the security and privilege attributes set on each channel has the security violation or the privilege violation, the bit of the channel number that violates security cannot be written or read, and the read value of the bit is 0.

Setting enable and disable bits for the same operation enable bit to 1 in the GTSECR is prohibited.

A bit written to 1 is automatically cleared. When the GTSECR is read, 0 is read.

Access in 8-bit or 16-bit units to the GTSECR register is prohibited, and it should be accessed in 32-bit units.

SBDCE bit (GTCCR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are enabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPE bit (GTPR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPDBR, and GTPBR registers are enabled.

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

SBDAE bit (GTADTR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[2] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTADTRA, GTADTBRA, and GTADTDBRA registers and using the GTADTRB, GTADTBRB, and GTADTDBRB registers are enabled.

Simultaneous setting of SBDAE and SBDAD bits to 1 is prohibited.

SBDDE bit (GTDV Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[3] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTDVU and GTDBU registers and using the GTDVD and GTDBD registers are enabled.

Simultaneous setting of SBDDE and SBDDD bits to 1 is prohibited.

SBDCD bit (GTCCR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are disabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPD bit (GTPR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPDBR, and GTPBR registers are disabled.

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

SBDAD bit (GTADTR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[2] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTADTRA, GTADTBRA, and GTADTDBRA registers and using the GTADTRB, GTADTBRB, and GTADTDBRB registers are disabled.

Simultaneous setting of SBDAE and SBDAD bits to 1 is prohibited.

SBDDD bit (GTDV Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[3] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTDVU and GTDBU registers and using the GTDVD and GTDBD registers are disabled.

Simultaneous setting of SBDDE and SBDDD bits to 1 is prohibited.

SPCE bit (Period Count Function Simultaneous Enable)

When 1 is written to this bit, 1 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is enabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

SSCE bit (Synchronous Set/Clear Simultaneous Enable)

When 1 is written to this bit, 1 is simultaneously set to GTCR.SSCEN bit in the channels set to 1 by the GTSECSR register and Enable synchronous set/clear function.

Simultaneous setting of SSCE and SSCD bits to 1 is prohibited.

SPCD bit (Period Count Function Simultaneous Disable)

When 1 is written to this bit, 0 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is disabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

SSCD bit (Synchronous Set/Clear Simultaneous Disable)

When 1 is written to this bit, 0 is simultaneously set to GTCR.SSCEN bit in the channels set to 1 by the GTSECSR register and Disable synchronous set/clear function.

Simultaneous setting of SSCE and SSCD bits to 1 is prohibited.

23.2.43 GTBER2 : General PWM Timer Buffer Enable Register 2

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xE0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	OLTTB[1:0]		OLTTA[1:0]		CPBTD	CP3DB	—		CPTDV	CPTADB	CPTADA	CPTPR	CPTCB	CPTCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CMTADB	CMTADA	—	CMTCB[1:0]		CMTCA[1:0]		—	—	CCTDV	CCTADB	CCTADA	CCTPR	CCTCB	CCTCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CCTCA	Counter Clear Source GTCCRA Register Buffer Transfer Disable 0: Enable GTCCRA register buffer transfer by counter clear 1: Disable GTCCRA register buffer transfer by counter clear	R/W

Bit	Symbol	Function	R/W
1	CCTCB	Counter Clear Source GTCCRB Register Buffer Transfer Disable 0: Enable GTCCRB register buffer transfer by counter clear 1: Disable GTCCRB register buffer transfer by counter clear	R/W
2	CCTPR	Counter Clear Source GTPR Register Buffer Transfer Disable 0: Enable GTPR register buffer transfer by counter clear 1: Disable GTPR register buffer transfer by counter clear	R/W
3	CCTADA	Counter Clear Source GTADTRA Register Buffer Transfer Disable 0: Enable GTADTRA register buffer transfer by counter clear 1: Disable GTADTRA register buffer transfer by counter clear	R/W
4	CCTADB	Counter Clear Source GTADTRB Register Buffer Transfer Disable 0: Enable GTADTRB register buffer transfer by counter clear 1: Disable GTADTRB register buffer transfer by counter clear	R/W
5	CCTDV	Counter Clear Source GTDVU/GTDVD Register Buffer Transfer Disable 0: Enable GTDVU/GTDVD register buffer transfer by counter clear 1: Disable GTDVU/GTDVD register buffer transfer by counter clear	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CMTCA[1:0]	Compare Match Source GTCCRA Register Buffer Transfer Enable 0 0: Disable GTCCRA register Buffer Transfer by compare match of GTCCRA register and GTCCRB register 0 1: Enable GTCCRA register Buffer Transfer by compare match of GTCCRA register 1 0: Enable GTCCRA register Buffer Transfer by compare match of GTCCRB register 1 1: Enable GTCCRA register Buffer Transfer by compare match of GTCCRA register and GTCCRB register	R/W
11:10	CMTCB[1:0]	Compare Match Source GTCCRB Register Buffer Transfer Enable 0 0: Disable GTCCRB register Buffer Transfer by compare match of GTCCRA register and GTCCRB register 0 1: Enable GTCCRB register Buffer Transfer by compare match of GTCCRA register 1 0: Enable GTCCRB register Buffer Transfer by compare match of GTCCRB register 1 1: Enable GTCCRB register Buffer Transfer by compare match of GTCCRA register and GTCCRB register	R/W
12	—	This bit is read as 0. The write value should be 0.	R/W
13	CMTADA	Compare Match Source GTADTRA Register Buffer Transfer Enable 0: Disable GTADTRA register buffer transfer by compare match of GTADTRA register 1: Enable GTADTRA register buffer transfer by compare match of GTADTRA register	R/W
14	CMTADB	Compare Match Source GTADTRB Register Buffer Transfer Enable 0: Disable GTADTRB register buffer transfer by compare match of GTADTRB register 1: Enable GTADTRB register buffer transfer by compare match of GTADTRB register	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
16	CPTCA	Overflow/Underflow Source GTCCRA Register Buffer Transfer Disable 0: Enable GTCCRA register buffer transfer by overflow/underflow 1: Disable GTCCRA register buffer transfer by overflow/underflow	R/W
17	CPTCB	Overflow/Underflow Source GTCCRB Register Buffer Transfer Disable 0: Enable GTCCRB register buffer transfer by overflow/underflow 1: Disable GTCCRB register buffer transfer by overflow/underflow	R/W
18	CPTPR	Overflow/Underflow Source GTPR Register Buffer Transfer Disable 0: Enable GTPR register buffer transfer by overflow/underflow 1: Disable GTPR register buffer transfer by overflow/underflow	R/W
19	CPTADA	Overflow/Underflow Source GTADTRA Register Buffer Transfer Disable 0: Enable GTADTRA register buffer transfer by overflow/underflow 1: Disable GTADTRA register buffer transfer by overflow/underflow	R/W
20	CPTADB	Overflow/Underflow Source GTADTRB Register Buffer Transfer Disable 0: Enable GTADTRB register buffer transfer by overflow/underflow 1: Disable GTADTRB register buffer transfer by overflow/underflow	R/W

Bit	Symbol	Function	R/W
21	CPTDV	Overflow/Underflow Source GTDVU/GTDVD Register Buffer Transfer Disable 0: Enable GTDVU/GTDVD register buffer transfer by overflow/underflow 1: Disable GTDVU/GTDVD register buffer transfer by overflow/underflow	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
24	CP3DB	Complementary PWM mode 3,4 Double Buffer select*1 0: Disable double buffer function in complementary PWM mode 3, 4 1: Enable double buffer function in complementary PWM mode 3, 4	R/W
25	CPBTD	Complementary PWM mode Buffer Transfer Disable*1 0: Enable buffer transfer from temporary register to GTCCRC and GTPBR register 1: Disable buffer transfer from temporary register to GTCCRC and GTPBR register	R/W
27:26	OLTTA[1:0]	GTIOCnA Output Level Buffer Transfer Timing Select*1 0 0: No transfer 0 1: Triangle waves, complementary PWM mode: Transfer at crest Saw waves: Transfer at the end of period 1 0: Triangle waves, complementary PWM mode: Transfer at trough Saw waves: Transfer by compare match of GTCCRA register 1 1: Triangle waves, complementary PWM mode: Transfer at both crest and trough Saw waves: Setting prohibited	R/W
29:28	OLTTB[1:0]	GTIOCnB Output Level Buffer Transfer Timing Select*1 0 0: No transfer 0 1: Triangle waves, complementary PWM mode: Transfer at crest Saw waves: Transfer at the end of period 1 0: Triangle waves, complementary PWM mode: Transfer at trough Saw waves: Transfer by compare match of GTCCRB register 1 1: Triangle waves, complementary PWM mode: Transfer at both crest and trough Saw waves: Setting prohibited	R/W
31:30	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323 and GPT3210 to GPT3213, this bit is read as 0. The write value should be 0.

The GTBER2 register makes settings for buffer operation.

Set the CP3DB bit and OLTTm[1:0] (m = A, B) bits when the GTCNT counter is stopped.

CCTCA bit (Counter Clear Source GTCCRA Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTCCRA, GTCCRC, and GTCCRD registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRA[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTCA bit is 0, buffer transfer is not performed by counter clear.

If there is a conflict with the CMTCA bit setting, the CCTCA bit setting has priority.

The setting is invalid during the event count operation.

CCTCB bit (Counter Clear Source GTCCRB Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTCCRB, GTCCRE, and GTCCRF registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRB[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTCB bit is 0, buffer transfer is not performed by counter clear.

If there is a conflict with the CMTCB bit setting, the CCTCB bit setting has priority.

The setting is invalid during the event count operation.

CCTPR bit (Counter Clear Source GTPR Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTPR, GTPBR, and GTPDBR registers together.

This bit is effective when the GTBER.BD[1] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.PR[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTPR bit is 0, buffer transfer is not performed by counter clear.

The setting is invalid during the event count operation.

CCTADm bit (Counter Clear Source GTADTRm Register Buffer Transfer Disable) (m = A, B)

This bit disables buffer transfer by counter clear using the GTADTRm, GTADTBRm and GTADTDBRm registers together.

This bit is effective when the GTBER.BD[2] bit is 0 (buffer operation enabled) and the buffer operation is selected by the ADTTm[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTADm bit is 0, buffer transfer is not performed by counter clear.

If there is a conflict with the CMTADm bit setting, the CCTADm bit setting has priority.

The setting is invalid during the event count operation.

CCTDV bit (Counter Clear Source GTDVU/GTDVD Register Buffer Transfer Disable)

This bit disables buffer transfer by counter clear using the GTDVU and GTDBU or GTDVD and GTDBD registers together.

This bit is effective when the GTBER.BD[3] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTDTCR.TDBUE or GTDTCR.TDBDE bit with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode. Even if the CCTDV bit is 0, buffer transfer is not performed by counter clear.

The setting is invalid during the event count operation.

CMTCA[1:0] bit (Compare Match Source GTCCRA Register Buffer Transfer Enable)

This bit enables buffer transfer by compare match of GTCCRA using the GTCCRA, GTCCRC, and GTCCRD registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRA[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

If there is a conflict with the CCTCA bit setting, the CCTCA bit setting has priority.

The setting is invalid during the event count operation.

CMTCB[1:0] bit (Compare Match Source GTCCRB Register Buffer Transfer Enable)

This bit enables buffer transfer by compare match of GTCCRB using the GTCCRB, GTCCRE, and GTCCRF registers together.

This bit is effective when the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRB[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

If there is a conflict with the CCTCB bit setting, the CCTCB bit setting has priority.

The setting is invalid during the event count operation.

CMTADm bit (Compare Match Source GTADTRm Register Buffer Transfer Enable) (m = A, B)

This bit enables buffer transfer by compare match of GTADTRm using the GTADTRm, GTADTBRm and GTADTDBRm registers together.

This bit is effective when the GTBER.BD[2] bit is 0 (buffer operation enabled) and the buffer operation is selected by the ADTTm[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

If there is a conflict with the CCTADm bit setting, the CCTADm bit setting has priority.

The setting is invalid during the event count operation.

CPTCA bit (Overflow/Underflow Source GTCCRA Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTCCRA, GTCCRC, and GTCCRD registers together.

This bit is effective when the CCTCA bit is 0 (GTCCRA register buffer transfer by counter clear is enabled), the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRA[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTCB bit (Overflow/Underflow Source GTCCRB Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTCCRB, GTCCRE and GTCCRF registers together.

This bit is effective when the CCTCB bit is 0 (GTCCRB register buffer transfer by counter clear is enabled), the GTBER.BD[0] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.CCRB[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTPR bit (Overflow/Underflow Source GTPR Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTPR, GTPBR, and GTPDBR registers together.

This bit is effective when the CCTPR bit is 0 (GTPR register buffer transfer by counter clear is enabled), the GTBER.BD[1] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTBER.PR[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTADm bit (Overflow/Underflow Source GTADTRm Register Buffer Transfer Disable) (m = A, B)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTADTRm, GTADTBRm and GTADTDBRm registers together.

This bit is effective when the CCTADm bit is 0 (GTADTRm register buffer transfer by counter clear is enabled), the GTBER.BD[2] bit is 0 (buffer operation enabled) and the buffer operation is selected by the ADTTm[1:0] bits with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CPTDV bit (Overflow/Underflow Source GTDVU/GTDVD Register Buffer Transfer Disable)

This bit disables buffer transfer by overflow/underflow in saw-waves using the GTDVU and GTDBU or GTDVD and GTDBD registers together.

This bit is effective when the CCTDV bit is 0 (GTDVU/GTDVD register buffer transfer by counter clear is enabled), the GTBER.BD[3] bit is 0 (buffer operation enabled) and the buffer operation is selected by the GTDTCR.TDBUE or GTDTCR.TDBDE bit with saw-waves.

The setting is invalid in triangle waves or complementary PWM mode.

The setting is invalid during the event count operation.

CP3DB bit (Complementary PWM mode 3,4 Double Buffer select)

This bit enables buffer transfer using the GTCCRA, GTCCRE and GTCCRF registers together in complementary PWM mode 3,4.

CPBTD bit (Complementary PWM mode Buffer Transfer Disable)

This bit disables buffer transfer from temporary register (temporary register A and temporary register P) to the GTCCRC and GTPBR registers during timer counting in complementary PWM mode 1, 2 and 3. When CP3DB bit is 1, the buffer

transfer from temporary register B to GTCCRE register is also disabled. The setting is invalid in complementary PWM mode 4.

OLTTm[1:0] bits (GTIOCnA Output Level Buffer Transfer Timing Select) (m = A, B)

This bit set the timing of buffer transfer from GTOLBR.GTIOmB[4:0] bits to GTIOR.GTIOm[4:0] bits.

23.2.44 GTOLBR : General PWM Timer Output Level Buffer Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xE4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	GTIOBB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	GTIOAB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOAB[4:0]	GTIOA buffer bits	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W
20:16	GTIOBB[4:0]	GTIOB buffer bits	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

The GTOLBR register is a buffer register for the GTIOR.GTIOA[4:0] bits and GTIOR.GTIOB[4:0] bits.

GTIOmB[4:0] bits (GTIOm buffer bits) (m = A, B)

These bits are buffer bits of GTIOR.GTIOm[4:0] bits.

These bits are transferred to the GTIOR.GTIOm[4:0] bits at the transfer timing selected by the GTBER2.OLTTm[1:0] (m = A, B) bits.

23.2.45 GTICCR : General PWM Timer Inter Channel Cooperation Input Capture Control Register

Base address: GPT32n = 0x4032_2000 + 0x0100 × n (n = 0 to 13)
GPT32n_NS = 0x5032_2000 + 0x0100 × n (n = 0 to 13)

Offset address: 0xEC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ICBGRP[1:0]		—	—	—	—	—	ICBCLK	ICBFPU	ICBFPO	ICBFF	ICBFE	ICBFD	ICBFC	ICBFB	ICBFA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ICAGRP[1:0]		—	—	—	—	—	ICACLK	ICAFPU	ICAFPO	ICAFF	ICAFE	ICAFD	ICAFC	ICAFB	ICAFA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICAFA	Forwarding GTCCRA register Compare Match/Input Capture to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRA register compare match/input capture to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRA register compare match/input capture to GTCCRA input capture source of other channels	R/W
1	ICAFB	Forwarding GTCCRB register Compare Match/Input Capture to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRB register compare match/input capture to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRB register compare match/input capture to GTCCRA input capture source of other channels	R/W
2	ICAFC	Forwarding GTCCRC register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRC register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRC register compare match to GTCCRA input capture source of other channels	R/W
3	ICAFD	Forwarding GTCCRD register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRD register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRD register compare match to GTCCRA input capture source of other channels	R/W
4	ICAFE	Forwarding GTCCRE register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRE register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRE register compare match to GTCCRA input capture source of other channels	R/W
5	ICAFF	Forwarding GTCCRF register Compare Match to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding GTCCRF register compare match to GTCCRA input capture source of other channels 1: Enable forwarding GTCCRF register compare match to GTCCRA input capture source of other channels	R/W
6	ICAFPO	Forwarding Overflow to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels 1: Enable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels	R/W
7	ICAFPU	Forwarding Underflow to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels 1: Enable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRA input capture source of other channels	R/W
8	ICACLK	Forwarding Count Clock to Other Channel GTCCRA Input Capture Source Enable 0: Disable forwarding count clock to GTCCRA input capture source of other channels 1: Enable forwarding count clock to GTCCRA input capture source of other channels	R/W
13:9	—	These bits are read as 0. The write value should be 0.	R/W
15:14	ICAGRP[1:0]	GTCCRA Input Capture Group Select 0 0: Select group A 0 1: Select group B 1 0: Select group C 1 1: Select group D	R/W

Bit	Symbol	Function	R/W
16	ICBFA	Forwarding GTCCRA register Compare Match/Input Capture to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRA register compare match/input capture to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRA register compare match/input capture to GTCCRB input capture source of other channels	R/W
17	ICBFB	Forwarding GTCCRB register Compare Match/Input Capture to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRB register compare match/input capture to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRB register compare match/input capture to GTCCRB input capture source of other channels	R/W
18	ICBFC	Forwarding GTCCRC register Compare Match to Other Channel GTCCRB Input Source Capture Enable 0: Disable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels	R/W
19	ICBFD	Forwarding GTCCRD register Compare Match to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRD register compare match to GTCCRB input capture source of other channels	R/W
20	ICBFE	Forwarding GTCCRE register Compare Match to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRE register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRE register compare match to GTCCRB input capture source of other channels	R/W
21	ICBFF	Forwarding GTCCRF register Compare Match to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding GTCCRF register compare match to GTCCRB input capture source of other channels 1: Enable forwarding GTCCRF register compare match to GTCCRB input capture source of other channels	R/W
22	ICBFPO	Forwarding Overflow to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels 1: Enable forwarding overflow in saw-waves or the crest in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels	R/W
23	ICBFPU	Forwarding Underflow to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels 1: Enable forwarding underflow in saw-waves or the trough in triangle-waves or complementary PWM mode to GTCCRB input capture source of other channels	R/W
24	ICBCLK	Forwarding Count Clock to Other Channel GTCCRB Input Capture Source Enable 0: Disable forwarding count clock to GTCCRB input capture source of other channels 1: Enable forwarding count clock to GTCCRB input capture source of other channels	R/W
29:25	—	These bits are read as 0. The write value should be 0.	R/W
31:30	ICBGRP[1:0]	GTCCRB Input Capture Group Select 0 0: Select group A 0 1: Select group B 1 0: Select group C 1 1: Select group D	R/W

The GTICCR register is a register that controls input capture by inter channel cooperation.

For channels that perform input capture by inter channel cooperation, the forwarding enable bit of the input capture source corresponding to the GTCCRA register or GTCCRB register where the input capture occurs is invalid.

ICAFm bit (Forwarding GTCCRm register Compare Match/Input Capture to Other Channel GTCCRA Input Capture Source Enable) (m = A, B)

Enables/disables the use of compare match/input capture of GTCCRm register as the input capture source of other channel's GTCCRA register.

ICAFx bit (Forwarding GTCCRx register Compare Match to Other Channel GTCCRA Input Capture Source Enable) (x = C, D, E, F)

Enables/disables the use of compare match of GTCCRx register as the input capture source of other channel's GTCCRA register.

ICAFPO bit (Forwarding Overflow to Other Channel GTCCRA Input Capture Source Enable)

Enable/disable to use the overflow of saw-waves, the crest of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRA register.

ICAFPU bit (Forwarding Underflow to Other Channel GTCCRA Input Capture Source Enable)

Enable/disable to use the underflow of saw-waves, the trough of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRA register.

ICACLK bit (Forwarding Count Clock to Other Channel GTCCRA Input Capture Source Enable)

Enable/disable to use count clock as the input capture source of other channel's GTCCRA register.

ICAGRP[1:0] bit (GTCCRA Input Capture Group Select)

Select the group of input capture by inter channel cooperation for GTCCRA register.

For channels that accept input capture of the GTCCRA register due to input capture sources from other channels, set the GTICASR.ASOC bit to 1 and select the group of inter channel cooperation with the ICAGRP[1:0] bits.

ICBFm bit (Forwarding GTCCRm register Compare Match/Input Capture to Other Channel GTCCRB Input Capture Source Enable) (m = A, B)

Enables/disables the use of compare match/input capture of GTCCRm register as the input capture source of other channel's GTCCRB register.

ICBFx bit (Forwarding GTCCRx register Compare Match to Other Channel GTCCRB Input Capture Source Enable) (x = C, D, E, F)

Enables/disables the use of compare match of GTCCRx register as the input capture source of other channel's GTCCRB register.

ICBFPO bit (Forwarding Overflow to Other Channel GTCCRB Input Capture Source Enable)

Enable/disable to use the overflow of saw-waves, the crest of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRB register.

ICBFPU bit (Forwarding Underflow to Other Channel GTCCRB Input Capture Source Enable)

Enable/disable to use the underflow of saw-waves, the trough of triangle-waves or complementary PWM mode as the input capture source of other channel's GTCCRB register.

ICBCLK bit (Forwarding Count Clock to Other Channel GTCCRB Input Capture Source Enable)

Enable/disable to use count clock as the input capture source of other channel's GTCCRB register.

ICBGRP[1:0] bit (GTCCRB Input Capture Group Select)

Select the group of input capture by inter channel cooperation for GTCCRB register.

For channels that accept input capture of the GTCCRB register due to input capture sources from other channels, set the GTICBSR.BSOC bit to 1 and select the group of inter channel cooperation with the ICBGRP[1:0] bits.

23.2.46 OPSCR : Output Phase Switching Control Register

Base address: GPT_OPS = 0x4032_3F00
GPT_OPS_NS = 0x5032_3F00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	Input Phase Soft Setting These bits set the input phase from software settings. Setting these bits is valid when OPSCR.FB = 1.	R/W
1	VF		R/W
2	WF		R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	U	Input U-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by GTCLK OPSCR.FB = 1 : Software settings (UF)	R
5	V	Input V-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by GTCLK OPSCR.FB = 1 : Software settings (VF)	R
6	W	Input W-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by GTCLK OPSCR.FB = 1 : Software settings (WF)	R
7	—	This bit is read as 0. The write value should be 0.	R/W
8	EN	Output Phase Enable 0: Do not output (Hi-Z external pin) 1: Output*1	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	FB	External Feedback Signal Enable This bit selects the input phase from software settings and external input. 0: Select the external input 1: Select the soft setting (OPSCR.UF, VF, WF)	R/W
17	P	Positive-Phase Output (P) Control 0: Level signal output 1: PWM signal output	R/W
18	N	Negative-Phase Output (N) Control 0: Level signal output 1: PWM signal output	R/W
19	INV	Output Phase Invert Control 0: Positive logic (active-high) output 1: Negative logic (active-low) output	R/W
20	RV	Output Phase Rotation Direction Reversal Control 0: Positive rotation 1: Reverse rotation	R/W
21	ALIGN	Input Phase Alignment 0: Input phase aligned to GTCLK 1: Input phase aligned to the falling edge of PWM	R/W

Bit	Symbol	Function	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disabled Source Selection 0 0: Select group A output disable source 0 1: Select group B output disable source 1 0: Select group C output disable source 1 1: Select group D output disable source	R/W
26	GODF	Group Output Disable Function 0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit*1	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFEN	External Input Noise Filter Enable 0: Do not use a noise filter on the external input 1: Use a noise filter on the external input	R/W
31:30	NFCS[1:0]	External Input Noise Filter Clock Selection Noise filter sampling clock setting of the external input. 0 0: GTCLK/1 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF , VF , WF bits (Input Phase Soft Setting)

The UF , VF , WF bits set the input phase from the software settings. When OPSCR.FB bit is 1, these bits are valid. The set value of the UF /VF /WF takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When the OPSCR.FB bit is 0, external inputs that are synchronized by GTCLK are monitored by these bits. When the OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF , OPSCR.VF , and OPSCR.WF bits.

EN bit (Output Phase Enable)

The EN bit controls the output enable signal of output phase (positive phase/negative phase).

When the OPSCR.EN bit is 1, the signal waveform is output.

When the OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF /VF /WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP[1:0], OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set the EN bit to 1. The EN bit should be set when output disable request does not occur from POEG. Also when OPSCR.GODF is 1 and the signal value selected in the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0. Even if 1 is written by software, the EN bit remains at 0.

For the return, after clearing the Output Disable Request by software, set the EN bit to 1.

Priority order of the EN bit is as follows (when the conflict occurs).

When writing 1 by software and clearing to 0 by the Output Disable Request conflict for the EN bit, clearing to 0 by the Output Disable Request is enabled.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output or PWM signal output for the positive-phase output (GTOUUP, GTOVUP and GTOWUP pins).

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output or PWM signal output for the negative-phase output (GTOULO, GTOVLO and GTOWLO pins).

INV bit (Output Phase Invert Control)

The INV bit selects one of the positive logic (active-high) output or negative logic (active-low) output for the output phase.

RV bit (Output Phase Rotation Direction Reversal Control)

The RV bit reverses the direction of rotation of the motor by inverting the input phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the GTCLK or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit).

When OPSCR.ALIGN bit is 0, input phase is aligned to GTCLK.

Note: When the chopping is performed, there are cases where the PWM width of output is shorter than the width of the PWM used to chop just before or after switching of output phase, depending on the phase difference between the phase output switch timing and the phase of PWM.

When OPSCR.ALIGN bit is 1, input phase is aligned with the falling edge of PWM.

GRP[1:0] bit (Output Disabled Source Selection)

The GRP[1:0] bit selects the output disable source.

The GRP bits should be set when GODF bit is 0. If GRP bits select a POEG except for the connected groups, the status of output pin never change to disable.

GODF bit (Group Output Disable Function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

When OPSCR.GODF bit is 0, this bit is ignored.

The GODF bit should be set when output disable request does not occur from POEG.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter for the external input is not used.

Note: Set this bit during the EN bit is 0 to avoid generation of unintentional internal edge caused by switching this bit.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit is 1, noise filter sampling clock setting of the external input is enabled.

1. Set the NFCS[1:0].
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

23.2.47 GTCLKCR : General PWM Timer Clock Control Register

Base address: GPT_GTCLK = 0x4032_3F10
GPT_GTCLK_NS = 0x5032_3F10

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPEN	Synchronization Circuit Bypass Enable 0: In case of using Bus Clock and GPT Core Clock asynchronously 1: In case of using Bus Clock and GPT Core Clock synchronously	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The GTCLKCR register is a register that controls the clock.

Set first of initial setting after resetting.

If MSTPCRE.MSTPE31 bit is 0, changing this register is prohibited.

BPEN bit (Synchronization Circuit Bypass Enable)

Enable or disable the synchronization bypass function between the bus clock (PCLKA) and GPT core clock (GTCLK).

Set 0 when using an asynchronous clock (GPTCLK) or 1 when using a synchronous clock (PCLKD) as the core clock.

23.3 Operation

23.3.1 Basic Operation

Each channel has a 32-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR or GTCCRm (m = A to F) controls the count cycle.

When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated GTIOCnA or GTIOCnB can be changed (n = 0 to 13). GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

23.3.1.1 Counter Operation

(1) Counter start and stop

The counter of each channel starts the count operation when GTCR.CST is set to 1, and stops counting when the bit is set to 0. The GTCR.CST bit value is changed by the following sources:

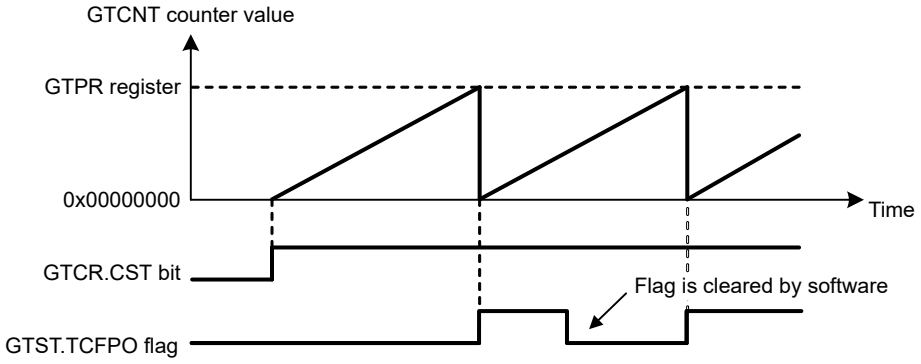
- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register

- Completion of the period count function while the GTPC.ASTP bit is 1

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with GTUPSR and GTDNSR registers set to 0x00000000. When the GTCNT value changes from the GTPR value to 0 (overflow) or the GTCCRm (m = A to F) value selected by the GTCSR.CSCMSC[2:0] bits to 0 in Saw-wave PWM mode 2, the overflow interrupt(GPTn_OVF) is also generated. After GTCNT overflows, up-counting resumes from 0x00000000.

Figure 23.5 shows an example of a periodic count operation in up-counting by the count clock.



Note: The base address of registers are the same.

Figure 23.5 Example of periodic count operation in up-counting by the count clock

Table 23.11 shows an example for setting periodic count operation in up-counting by the count clock.

Table 23.11 Example for setting a periodic count operation in up-counting by the count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.5, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.5, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 23.5, 0x00000000 is set.
6	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with GTUPSR and GTDNSR registers set to 0x00000000. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1, and the underflow interrupt(GPTn_UDF) is also generated. After the GTCNT counter underflows, down-counting resumes from the GTPR value.

Figure 23.6 shows an example of periodic count operation in down-counting by the count clock.

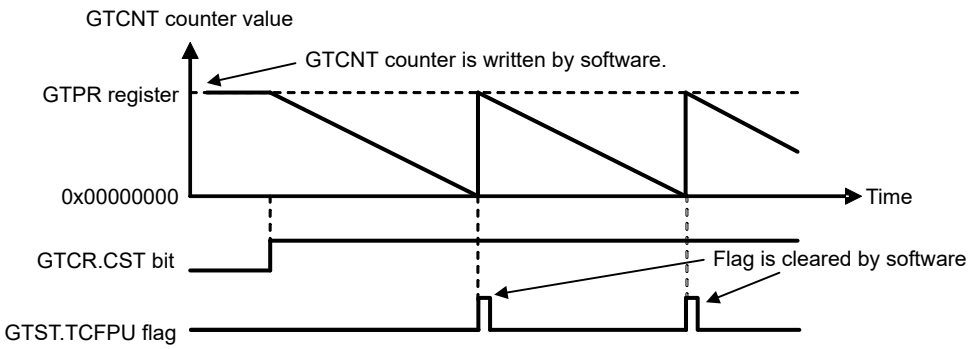


Figure 23.6 Example of periodic count operation in down-counting by the count clock

Table 23.12 shows an example for setting periodic count operation in down-counting by the count clock.

Table 23.12 Example for setting periodic count operation in down-counting by count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.6, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction with the GTUDDTYC register. In Figure 23.6, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 23.6, the GTPR register value is set.
6	Start count operation	Set the GTCR.CST bit to 1 to start count operation. In Figure 23.6, 1 is set in the CST bit.

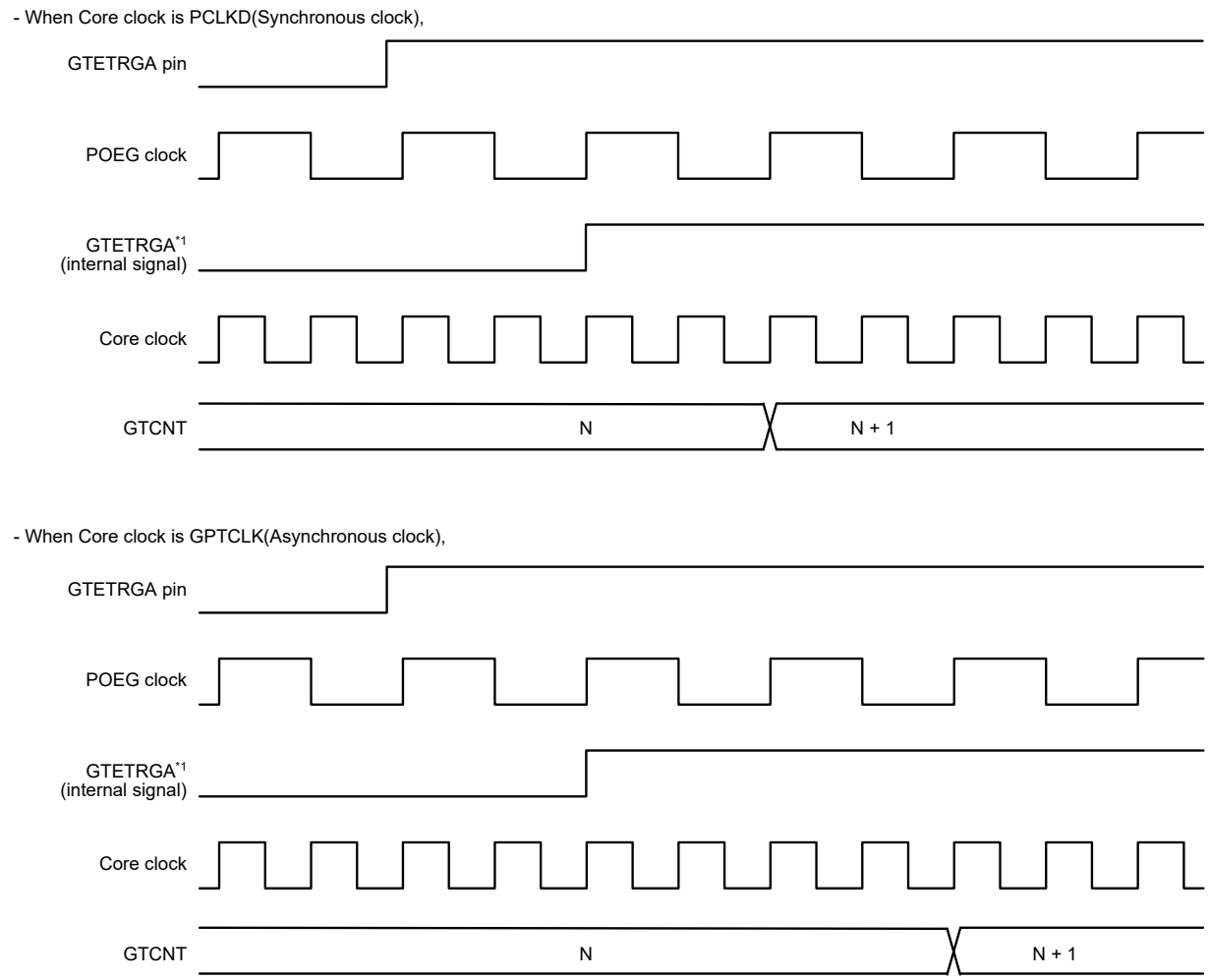
(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior when up-counting using hardware sources is the same as when up-counting by the count clock.

If you are using a hardware source to count up, set the GTCR.CST bit to 1 to enable the counting operation. After GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized by the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count up with a 1 GTCLK delay after GTCR.CST is set to 1.

Figure 23.7 shows an example of an event count operation in up-counting by a hardware resource (the rising edge of GTETRGA pin input).



Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 23.7 Example of event count operation in up-counting using hardware sources

Figure 23.8 shows an example of event count operation by ELC_GPTA event input.

This is an example of event count operation of GPT321.GTCNT counter. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

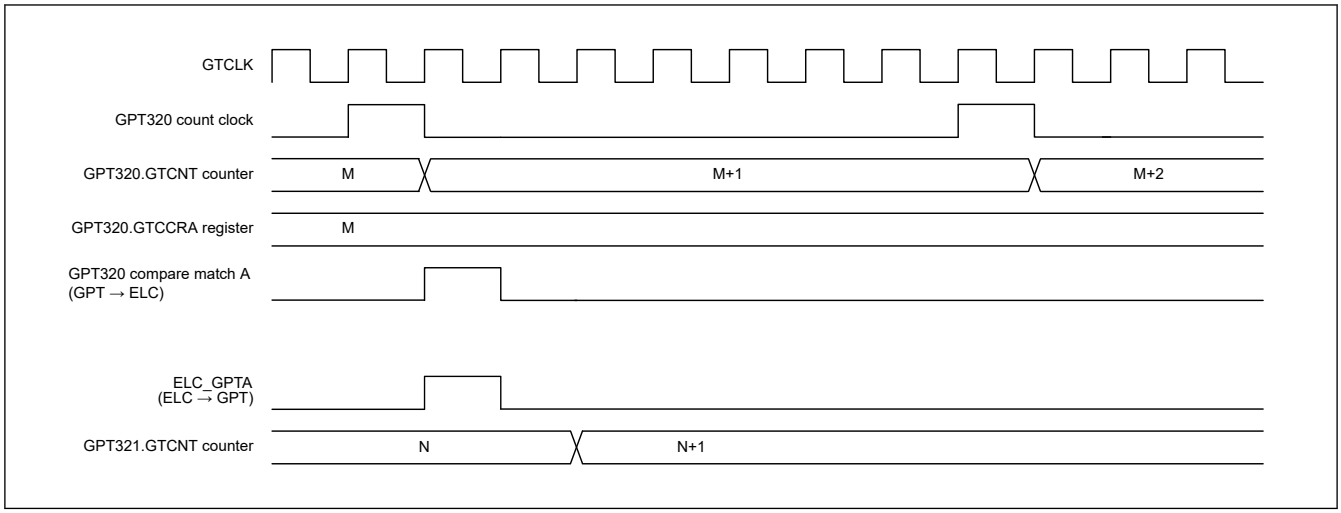


Figure 23.8 Example of Event Count Operation (Up-Counting the Number of Event Signals Input from ELC_GPTA)

Table 23.13 shows an example for setting event count operation in up-counting by a hardware source.

Table 23.13 Example for setting an event count operation in up-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-up hardware source with the GTUPSR register.
2	Set cycle	Set the cycle in the GTPR register.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

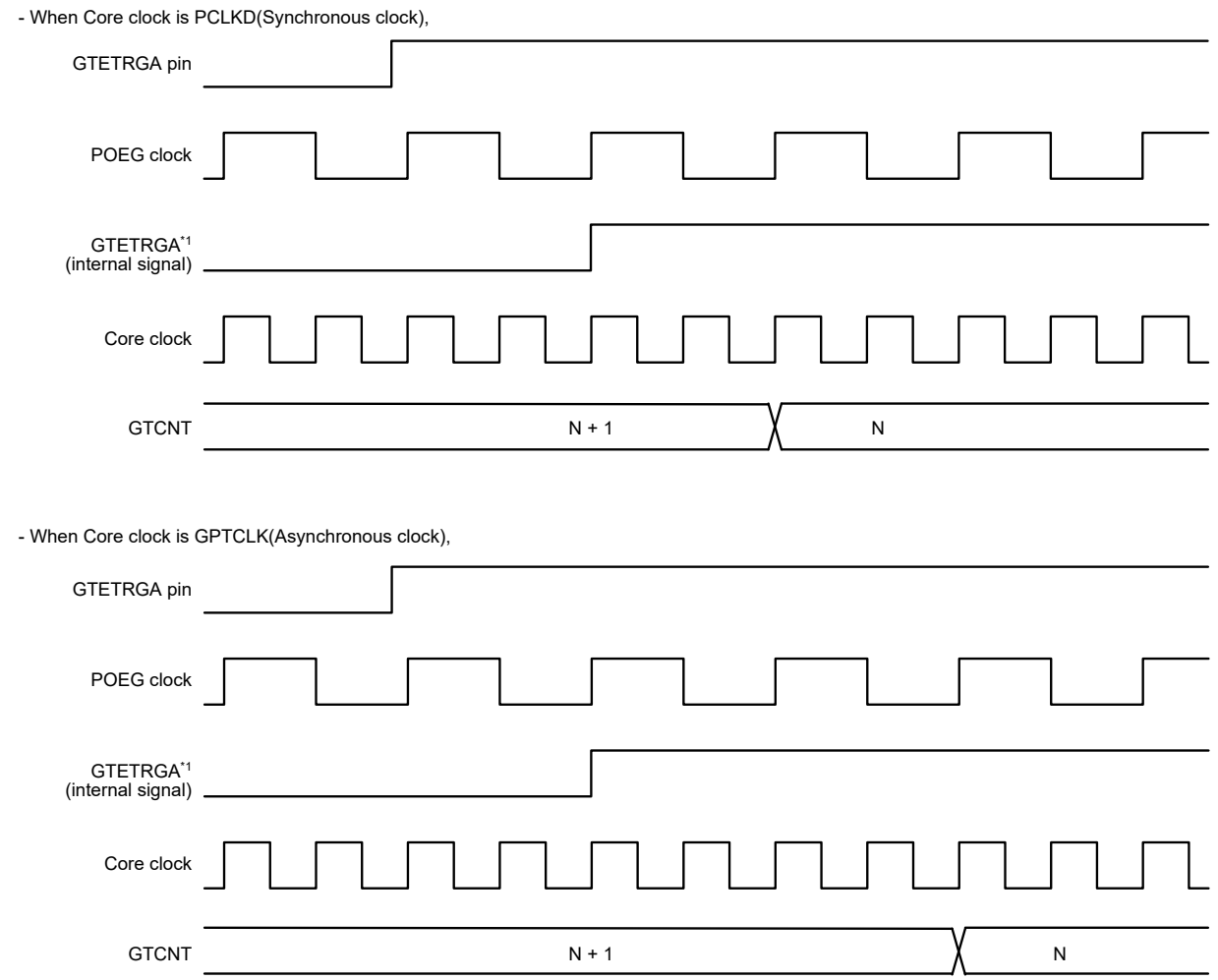
(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The underflow behavior when down-counting using hardware sources is the same as when down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized with the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count down with a 1 GTCLK delay after GTCR.CST is set to 1.

Figure 23.9 shows an example of a event count operation in down-counting by a hardware resource (rising edge of GTETRGA pin).



Note: POEG clock: PCLKB
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 23.9 Example of event count operation in down-counting using hardware sources

Table 23.14 shows an example for setting a periodic count operation in down-counting using a hardware resource.

Table 23.14 Example for setting an event count operation in down-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-down hardware source with the GTDNSR register.
2	Set cycle	Set the cycle in the GTPR register.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

(6) Counter clear operation

The counter of each channel is cleared by following sources:

- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit set to 1
- The hardware source selected in GTCSR register.

Write access during counting (when CST = 1) is disabled. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST is 1) or not (GTCR.CST is 0).

When the count direction flag is set as decrement (GTST.TCUF flag = 0) in saw-wave mode (Except saw-wave PWM mode 2) selected with GTCR.MD[2:0] bits or GTCR.MD[3:0] bits, the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

When not in saw-waves mode (except saw-wave PWM mode 2) and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

In event count operation when at least 1 bit in the GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to GTCLR register and clearing by hardware sources are performed immediately to synchronize with GTCLK. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[3:0].

23.3.1.2 Waveform Output by Compare Match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. At the same time, the GPT can output low, high, or toggled output from the associated GTIOCnA or GTIOCnB output pin (n = 0 to 13). In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the cycle end which is determined by GTPR or GTCCRm selected as a counter clear source by the GTCSR.CSCMSC[2:0] bits in saw-wave PWM mode 2 (n = 0 to 13, m = A to F).

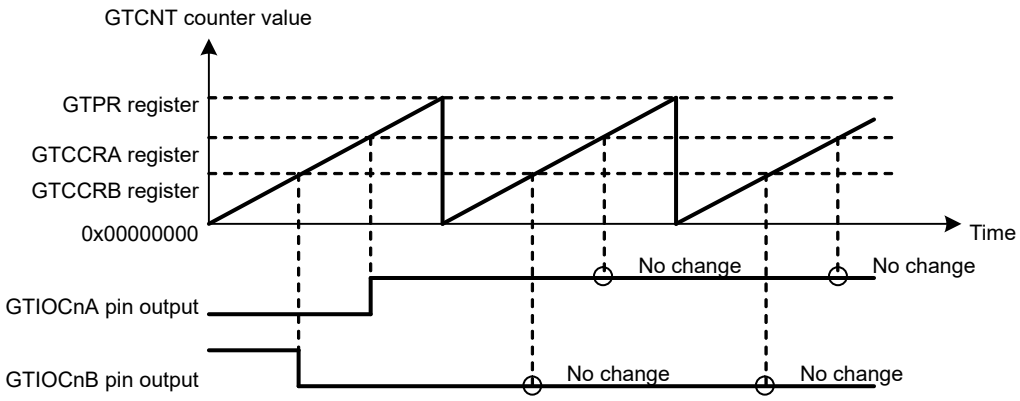
The cycle end is:

- For saw waves (except saw-wave PWM mode 2) in up-counting – when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves (except saw-wave PWM mode 2) in down-counting – when GTCNT changes from 0 to GTPR value (underflow)
- For saw-wave PWM mode 2 and GTCCRm register (m = A to F) selected as a counter clear source by the GTCSR.CSCMSC[2:0] bits – When the GTCNT counter value changes from the GTCCRm register value to 0x0000 0000
- For saw waves – when the GTCNT counter is cleared
- For triangle waves or complementary PWM mode – when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 23.10 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOCnA pin by a GTCCRA compare match, and low is output from the GTIOCnB pin by a GTCCRB compare match. The pin level does not change when the specified level and pin level match.



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is low, high output at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is high, low output at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 23.10 Example of low output and high output operation

Table 23.15 shows an example for setting low output and high output operation.

Table 23.15 Example for setting low output and high output operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.10, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.10, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.10, GTIOA[4:0] = 00010b, GTIOB[4:0] = 10001b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value*1	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

Note: n: 0 to 13
m: A, B

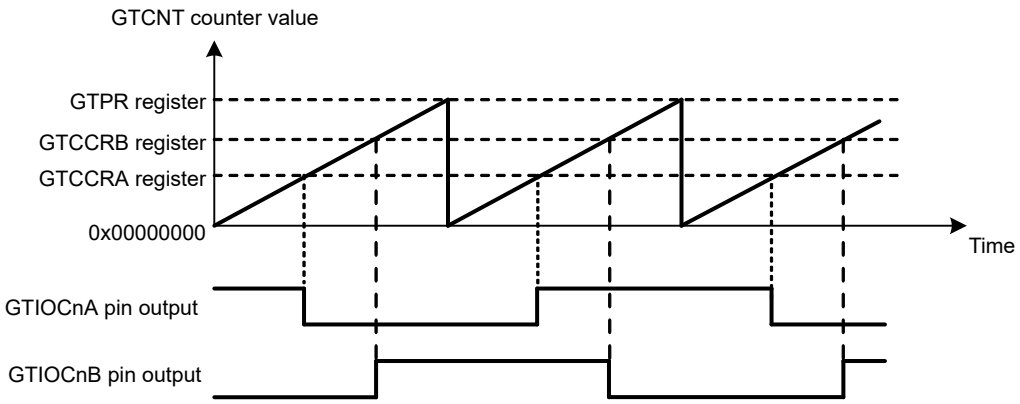
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

(2) Toggled output

Figure 23.11 and Figure 23.12 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB.

In Figure 23.11, the GTCNT counter performs up-counting, and settings are made so that the GTIOCnA pin output by a GTCCRA compare match and GTIOCnB pin output by a GTCCRB compare match are toggled.

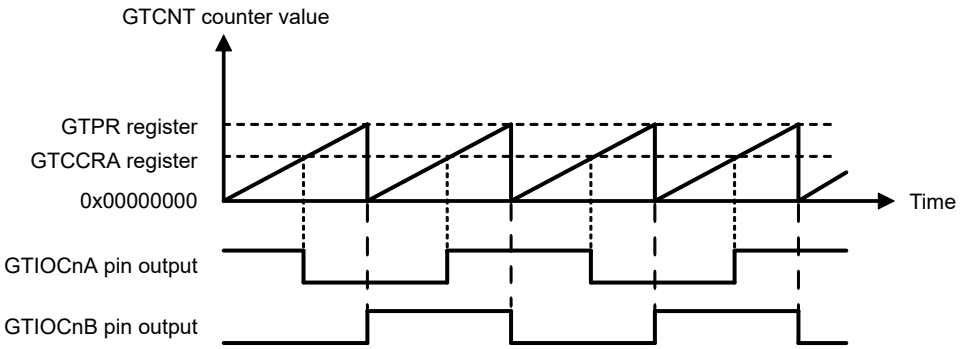
In Figure 23.12, the GTCNT counter performs up-counting, and settings are made so that a GTCCRA compare match toggles the GTIOCnA pin output level and a cycle end toggles the GTIOCnB pin output level.



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output toggled at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 23.11 Example of toggled output operation (1)



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output retained at compare match, output toggled at cycle end

Note: The base address of registers are the same.

Figure 23.12 Example of toggled output operation (2)

Table 23.16 shows an example for setting toggled output operation.

Table 23.16 Example for setting toggled output operation (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.11 and Figure 23.12, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.11 and Figure 23.12, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.

Table 23.16 Example for setting toggled output operation (2 of 2)

No.	Step Name	Description
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.11, GTIOA[4:0] = 10011b, GTIOB[4:0] = 00011b, and in Figure 23.12, GTIOA[4:0] = 10011b, GTIOB[4:0] = 01100b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value*1	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

Note: n: 0 to 13
m: A, B

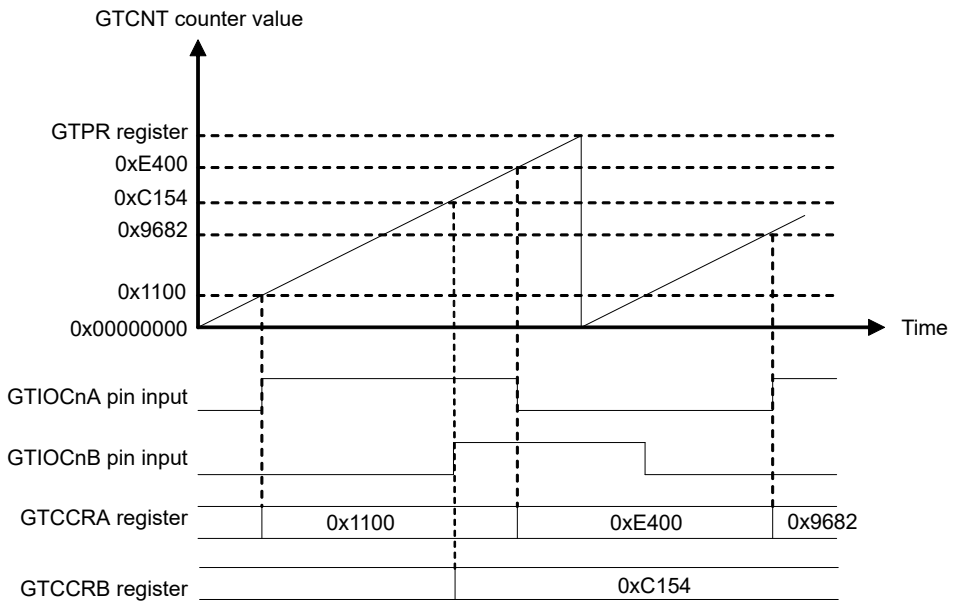
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

23.3.1.3 Input Capture Function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR. In complementary PWM mode, GTCCRA and GTCCRB registers do not function as input capture registers.

Figure 23.13 shows an example of the input capture function.

In this example, the GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTCCRA at both edges of the GTIOCnA input pin and to GTCCRB on the rising edge of the GTIOCnB input pin.



Note: The base address of registers are the same.
Note: [Setting examples]
GTICASR setting: input capture at both edges
GTICBSR setting: input capture at the rising edge

Figure 23.13 Example of input capture operation

Table 23.17 and Table 23.21 show the example for setting an input capture operation with count operation by the count clock.

Table 23.17 Example for setting input capture operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.13, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.13, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select the input capture source in the GTICASR and GTICBSR registers. In Figure 23.13, GTICASR = 0x00000F00, GTICBSR = 0x00003000. In GPT324 to GPT329 when input capture by other channel sources is used, set the GTICmSR.mSOC bit (m = A or B) to 1 and allow input capture by other channel sources, and select the group that cooperates with other channel sources by the GTICCR register.
7	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

Figure 23.14 shows an example of the timing of input capture operation in response to ELC_GPTA event input.

This is an example of capture of the counter value by the GPT321.GTCCRA register in response to an input signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

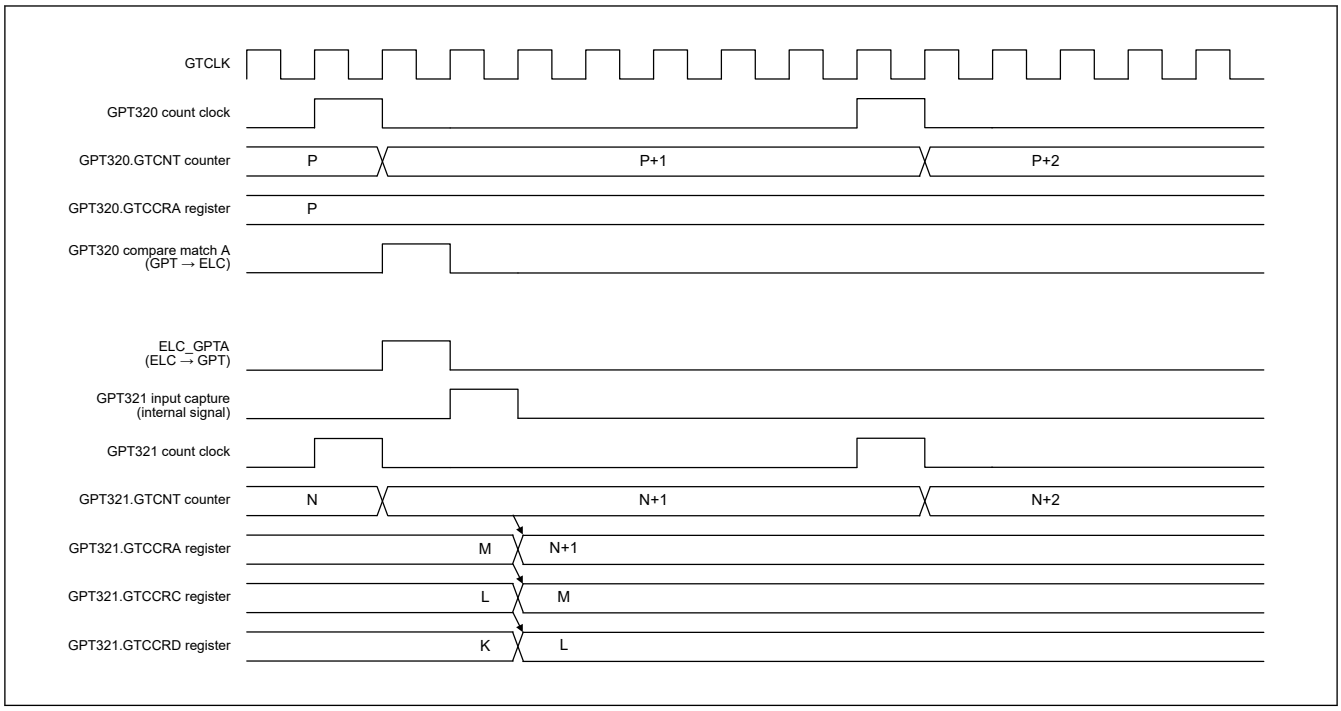


Figure 23.14 Example of the Timing of Input Capture Operation in Response to ELC_GPTA Event Input

Figure 23.15 shows an example of the timing of input capture operation in response to count clock from other channel.

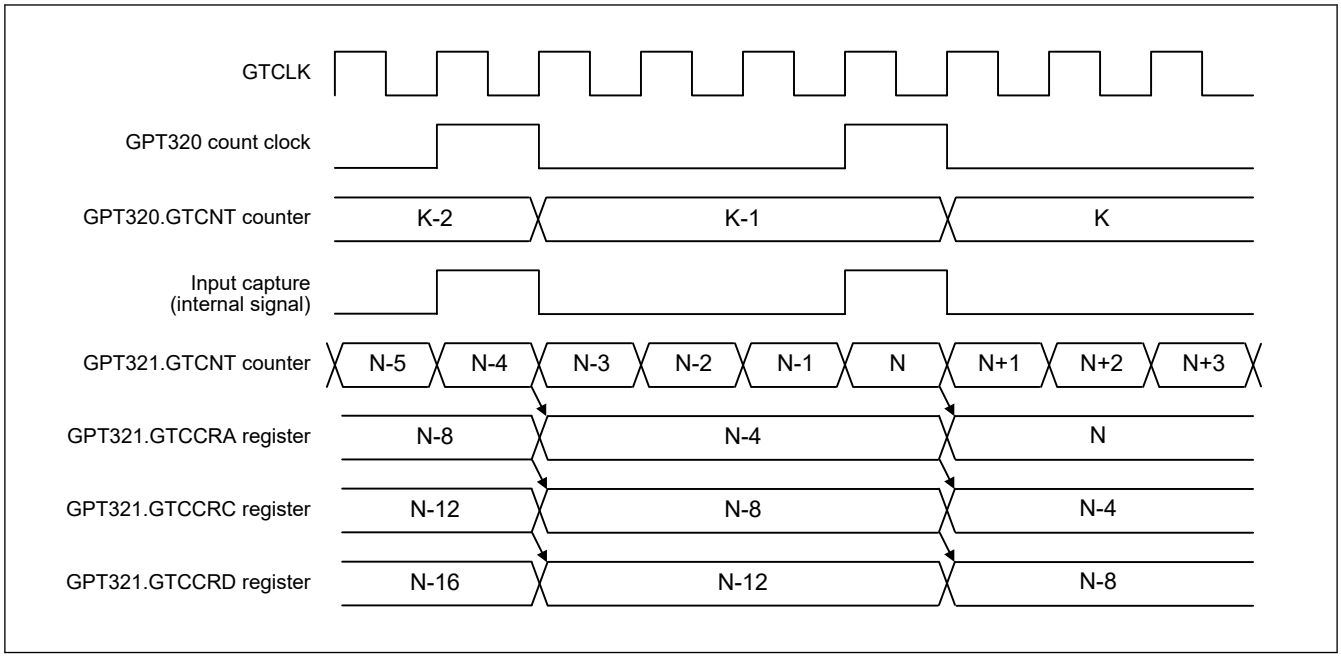


Figure 23.15 Example of the Timing of Input Capture Operation in Response to Count Clock from Other Channel

23.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- GTPR, GTPBR, and GTPDBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF
- GTADTRA, GTADTBRA, and GTADTDBRA
- GTADTRB, GTADTBRB, and GTADTDBRB

The following buffer operation is enabled by setting GTDTCR:

- GTDVU and GTDBU
- GTDVD and GTDBD

The following buffer operation is enabled by setting GTBER2:

- GTCCRA, GTCCRE, and GTCCRF (in complementary PWM mode 3, 4)
- GTOLBR.GTIOAB[4:0] bits and GTIOR.GTIOA[4:0] bits
- GTOLBR.GTIOBB[4:0] bits and GTIOR.GTIOB[4:0] bits

23.3.2.1 GTPR Register Buffer Operation

GTPBR can function as a buffer register for GTPR.

GTPDBR register can function as a buffer register for the GTPBR register (double-buffer register for the GTPR register).

In complementary PWM mode, the buffer transfer from the GTPDBR register to temporary register P is performed only in the master channel (GPT32n). The temporary register P is transferred to each GTPBR register of master channel, slave channel 1 (GPT32n+1), and slave channel 2 (GPT32n+2). Transfer from the GTPBR register to the GTPR register is made concurrently in three channels. Therefore, the same value is stored in the same register of the three channels. The GTPR register of the master channel represents the GTCNT counter's (GTCNTn) period of the master channel. In the slave channels, periods are controlled using the GTPR register value and the GTDVU register value.

The setting is invalid in the Saw-wave PWM mode 2.

The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in GTCSR register)
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR.CCLRn bit is set to 1, n = 0 to 13).

In the case of saw waves, the buffer transfer by clearing counter can be prohibited by GTBER2.CCTPR bit.

Table 23.18 shows the buffer transfer timing in the complementary PWM mode.

Table 23.18 GTPR Buffer Transfer Timing in Complementary PWM Mode

	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3, 4
GTPDBR ↓ Temporary register P	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register P ↓ GTPBR	(1) When data is transferred to temporary register P during up-counting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than up-counting middle section: At the end of trough section	(1) When data is transferred to temporary register P during down-counting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than down-counting middle section: At the end of crest section	(1) When data is transferred to temporary register P during middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than middle section: At the end of crest/ trough sections
GTPBR ↓ GTPR	At the end of crest section At the end of crest section Synchronous Counter clear in up counting middle section and crest section (Including counter clear by setting GTCSR.CP1CCE)	At the end of trough section Counter clear in down counting middle section and trough section	At the end of crest section At the end of trough section Counter clear

To set GTPR to function as a buffer, set the GTBER.PR bit to 1. To set GTPR not to function as a buffer, set the GTBER.PR bit to 0.

To set the GTPR register to function as double buffer, set the GTBER.PR[1:0] bits to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.

In complementary PWM mode, complementary PWM mode-specific buffer operation is performed regardless of the GTBER.PR[1:0] bit setting.

Figure 23.16 to Figure 23.21 show examples of GTPR buffer operation and Table 23.19 shows an example for setting GTPR buffer operation. For details of operation settings in complementary PWM mode, see section 23.3.3.7. Complementary PWM mode 1, 2, 3.

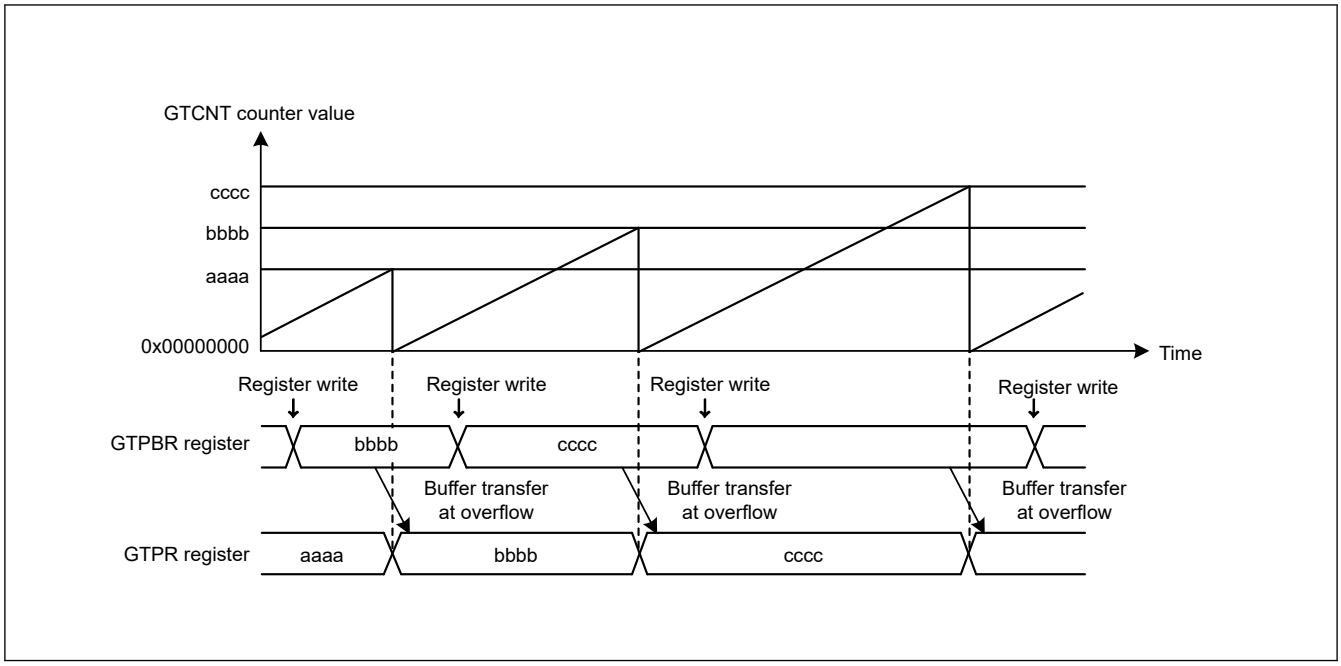


Figure 23.16 Example of GTPR buffer operation with saw waves in up-counting

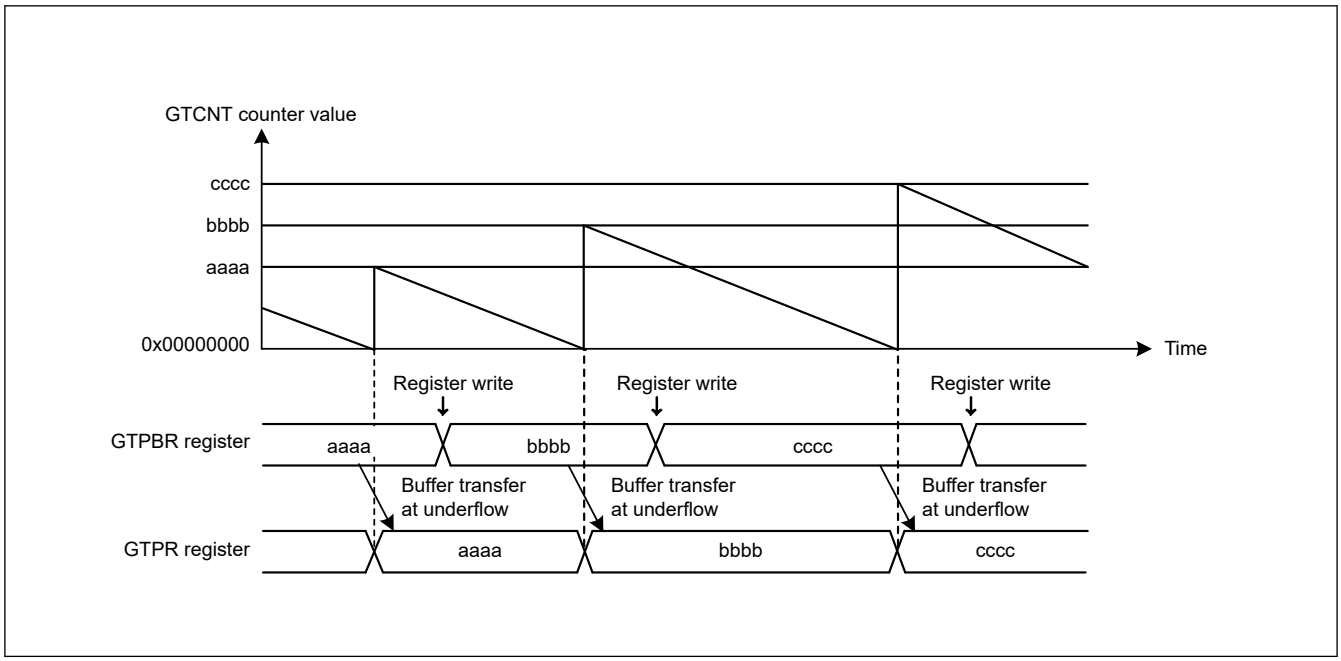


Figure 23.17 Example of GTPR buffer operation with saw waves in down-counting

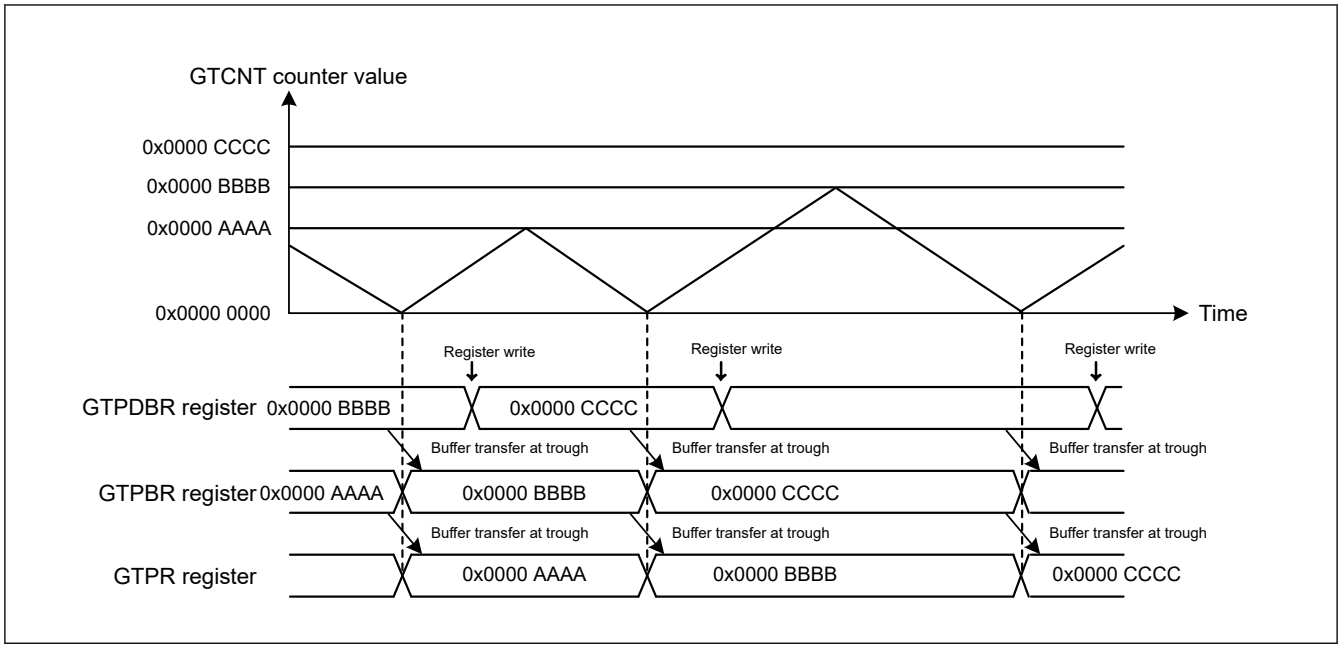


Figure 23.18 Example of GTPR double buffer operation with triangle waves

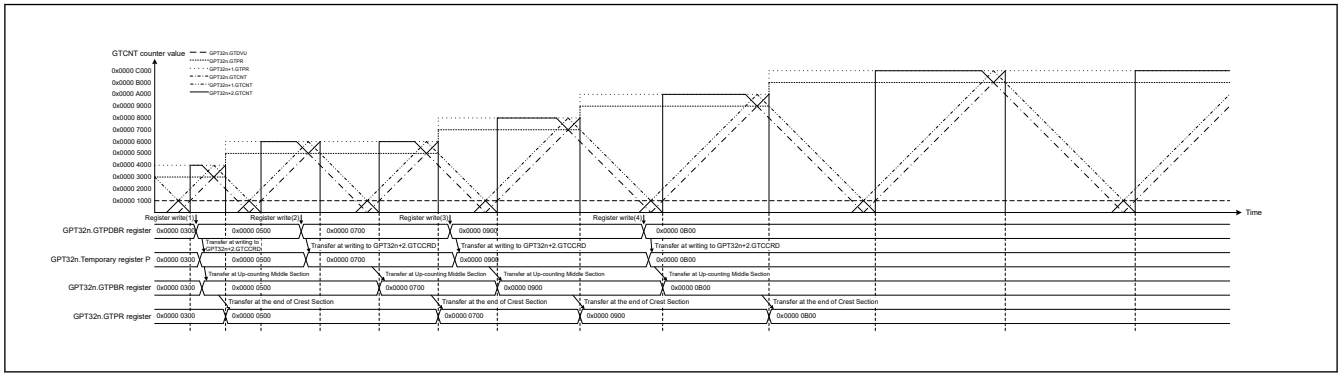


Figure 23.19 Example of GTPR double buffer operation with complementary PWM mode 1

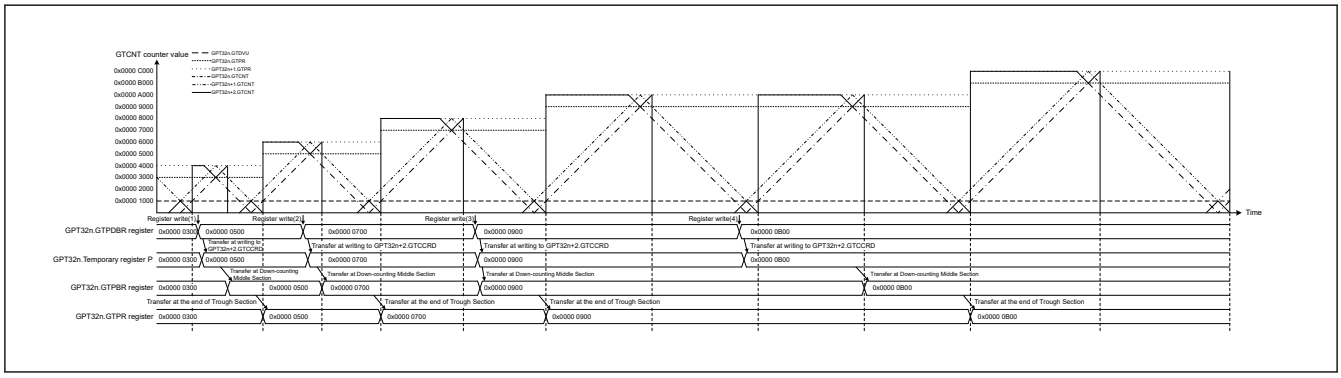


Figure 23.20 Example of GTPR double buffer operation with complementary PWM mode 2

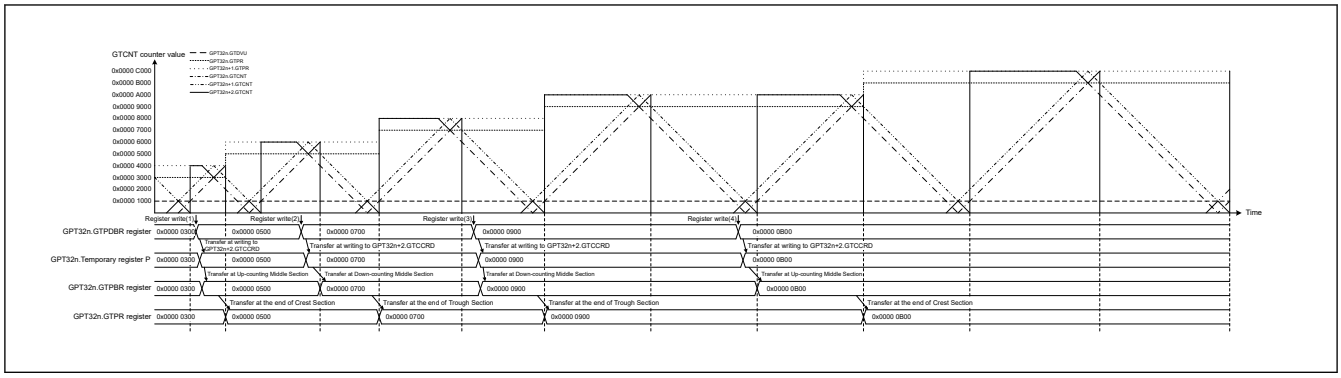


Figure 23.21 Example of GTPR double buffer operation with complementary PWM mode 3, 4

Table 23.19 Example for setting GTPR register buffer operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.16 and Figure 23.17, 000b or 0000b (saw-wave PWM mode 1) is set, and in Figure 23.18, 100b or 0100b (triangle-wave PWM mode 1) is set. In Figure 23.19 to Figure 23.21, 11xxb (complementary PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.16, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting). In Figure 23.17, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with the GTBER.PR[1:0] bits. In Figure 23.16 and Figure 23.17, PR[1:0] = 01b. In Figure 23.18, PR[1:0] = 1xb. In Figure 23.19 to Figure 23.21, no PR[1:0] bits setting required.
7	Set buffer value	For buffer operation, set a value in one cycle after the current cycle in the GTPBR register. For double buffer operation, also set a value of the period for the cycle after the next cycle in the GTPDBR register.
8	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
9	Set buffer value for each cycle	For buffer operation, set a value in one cycle after the current cycle in the GTPBR register. For double buffer operation, also set a value of the period for the cycle after the next cycle in the GTPDBR register. In complementary PWM mode 1 (crest transfer), when the GTPDBR register is set in the up-counting trough or middle section, a value of the period for the next cycle is set. In other sections, a value of the period for the cycle after the next cycle is set. In complementary PWM mode 2 (trough transfer), when the GTPDBR register is set in the up-counting sect ion or the down-counting crest or middle sections, a value of the period for the next cycle is set. In other sections, a value of the period for the cycle after the next cycle is set. In complementary PWM mode 3 or 4 (crest/trough immediate transfer), when the GTPDBR register is set in a section other than the down-counting trough section, a value of the period for the next cycle is set. In the down-counting trough section, a value of the period for the cycle after the next cycle is set.

23.3.2.2 Buffer Operation for GTCCRA and GTCCRB Registers

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. To set GTCCRA or GTCCRB to not function as a buffer, set 00b.

In saw-wave one-shot pulse mode, triangle-wave PWM mode 3, complementary PWM mode, the buffer operations that specific each PWM output operation mode are performed regardless of the setting of GTBER.CCRA [1:0] bits and GTBER.CCRB [1:0] bits.

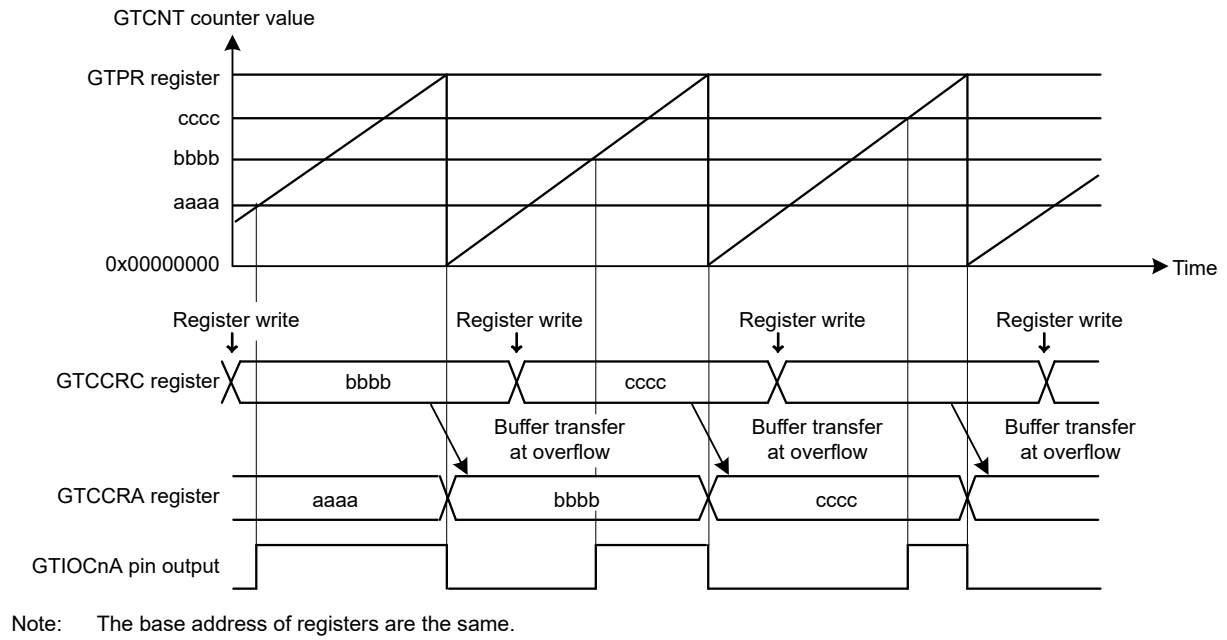
(1) When GTCCRA or GTCCRB Functions as Output Compare Register

In saw-wave one-shot pulse mode, triangle-wave PWM mode 3, complementary PWM mode, the buffer operations that specific each PWM output operation mode are performed regardless of the setting of GTBER.CCRA [1:0] bits and GTBER.CCRB [1:0] bits. For details, see section 23.3.3. PWM Output Operating Mode. Other than the specified PWM output operation mode, buffer transfer occurs in the following situations:

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear
  In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources similar to the case shown in section 23.3.2.1. GTPR Register Buffer Operation.
  In saw-wave, the buffer transfer of GTCCRm register by counter clearing is possible to be disabled with GTBER2.CCTCm bit (m = A, B).
  In triangle-wave mode, buffer transfer is not performed by the counter clear.
- Buffer transfer by compare match
  In saw-wave, the buffer transfer by the compare match of GTCCRm register enabled by GTBER2.CMTCm (m = A, B) bit is performed.
- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfer are performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode. Additionally, buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3.

When the setting of the GTBER.DBRTECm (m = A, B) bit is 1 in saw-wave one-shot pulse mode or triangle-wave PWM mode 3, transfer from the intermediate buffers to the GTCCRm (m = A, B) registers is repeated on a cyclic basis even while buffer transfer is disabled by the setting of the GTBER.BD[0] bit or buffer transfer extended skipping function (function for repeated double-buffer operation while buffer transfer is disabled). For details, see section 23.8.2.2. Repeated Double-Buffered Operation When Disabling GTCCR Buffer Transfer.

Figure 23.22 to Figure 23.25 show examples of GTCCRA and GTCCRB buffer operation and Table 23.20 shows an example for setting GTCCRA and GTCCRB buffer operation.



Note: The base address of registers are the same.

Figure 23.22 Example of GTCCRA and GTCCRB buffer operation with output compare, Saw-wave PWM mode 1 in up- counting, high output at GTCCRA compare match, and low output at cycle end

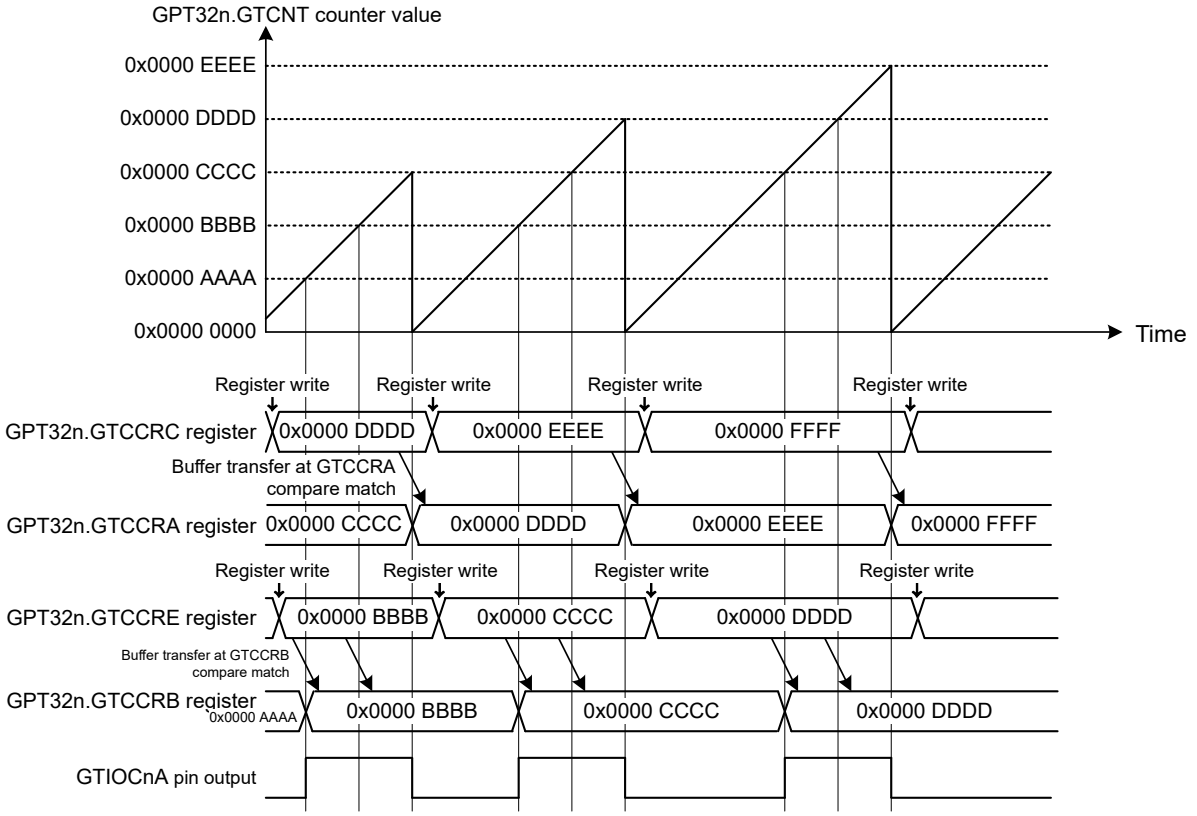
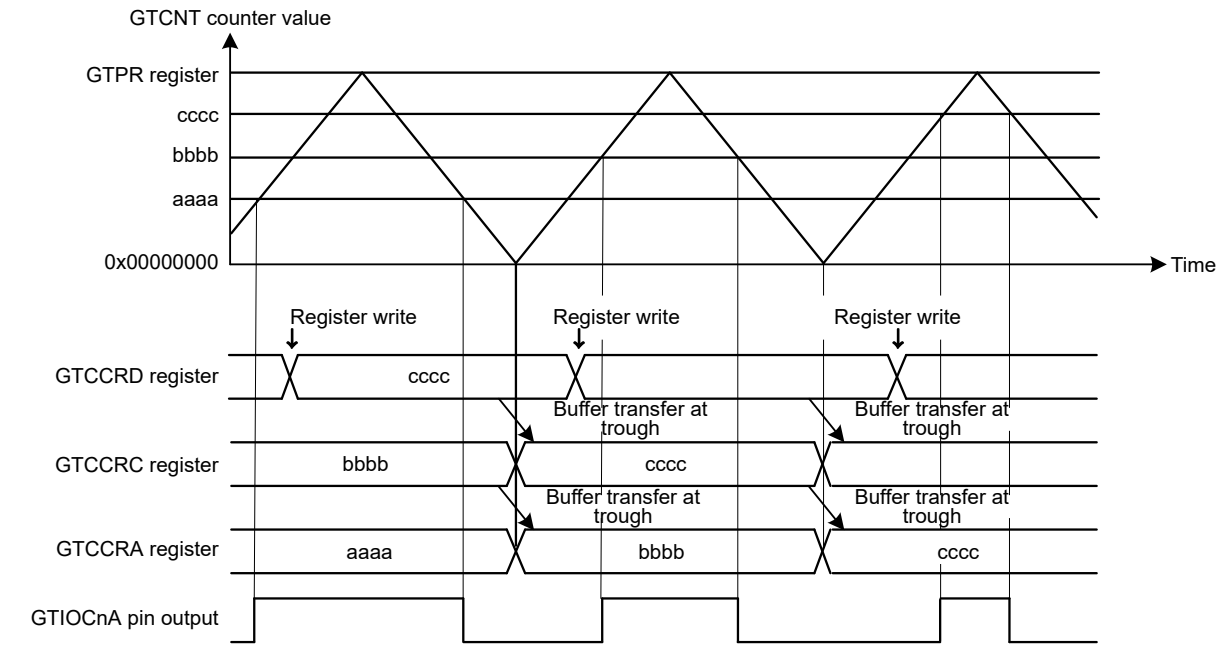
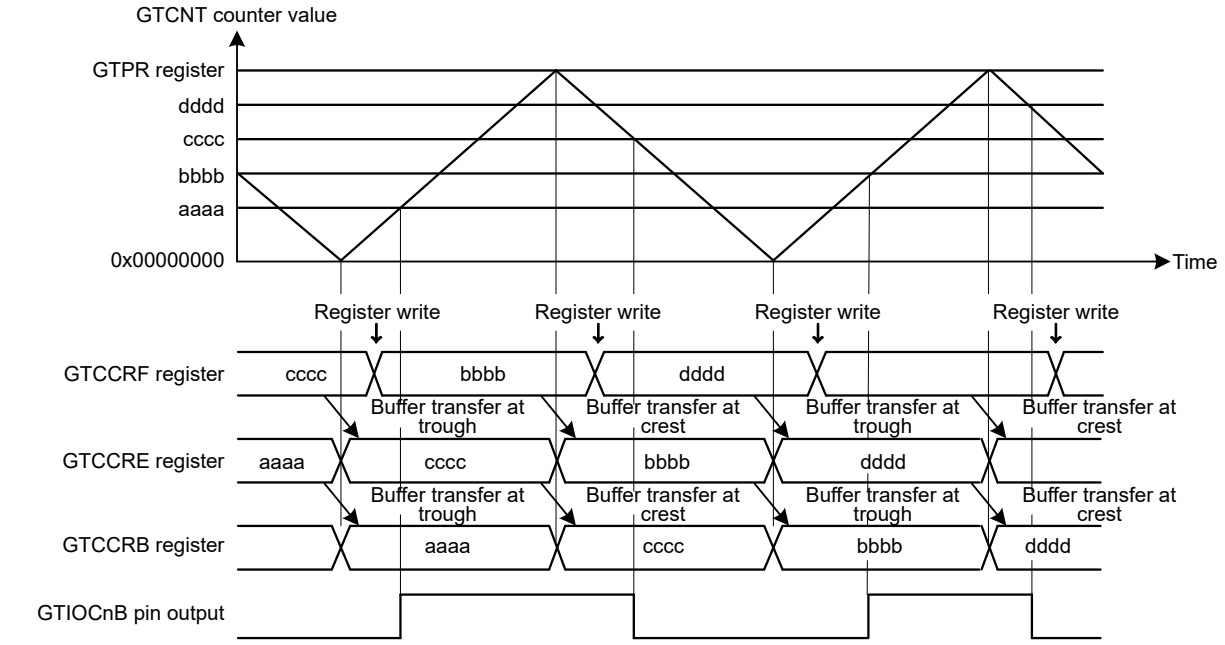


Figure 23.23 Example of GTCCRA and GTCCRB Registers Buffer Operation (Output Compare, Saw-Wave PWM Mode 2, Buffer Transfer at GTCCRA Register Compare Match, Counter Clearing, Low Output, Buffer Transfer at GTCCRB Register Compare Match, High Output) (n = 4 to 9)



Note: The base address of registers are the same.

Figure 23.24 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end



Note: The base address of registers are the same.

Figure 23.25 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end

Table 23.20 Example for setting GTCCRA and GTCCRB buffer operation for output compare

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.22, 000b or 0000b (saw-wave PWM mode 1) is set, in Figure 23.23, 0010b (saw-wave PWM mode 2) is set, in Figure 23.24, 100b or 0100b (triangle-wave PWM mode 1) is set, and in Figure 23.25, 101b or 0101b (triangle-wave PWM mode 2) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.22, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.22, GTIOA[4:0] = 00110b, in Figure 23.23, GTIOA[4:0] = 00101b and GTIOB[1:0] = 10b, in Figure 23.24, GTIOA[4:0] = 00011b, and in Figure 23.25, GTIOB[4:0] = 00011b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 23.22, CCRA[1:0] = 01b, in Figure 23.23, CCRA[1:0] = 01b and CCRB[1:0] = 01b, in Figure 23.24, CCRA[1:0] = 1xb, and in Figure 23.25, CCRB[1:0] = 1xb.
9	Set compare match value*1	Set the GTIOCnA pin transition in the GTCCRA register and the GTIOCnB pin transition in the GTCCRB register.
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTCCRD and GTCCRF registers, respectively.

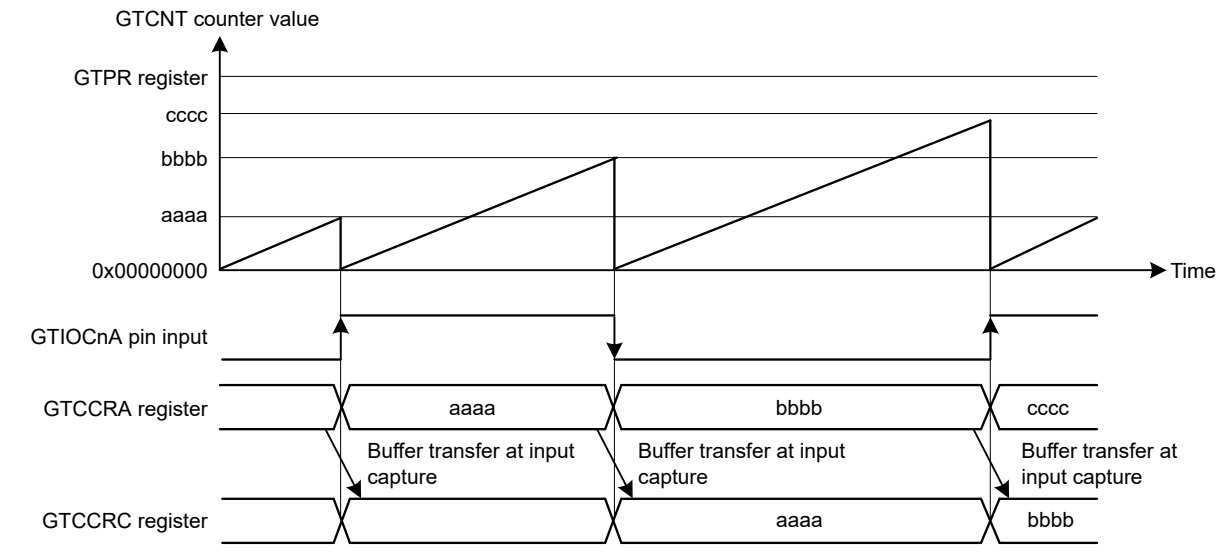
Note: n: 0 to 13
m: A, B

Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

(2) When GTCCRA or GTCCRB Functions as Input Capture Register

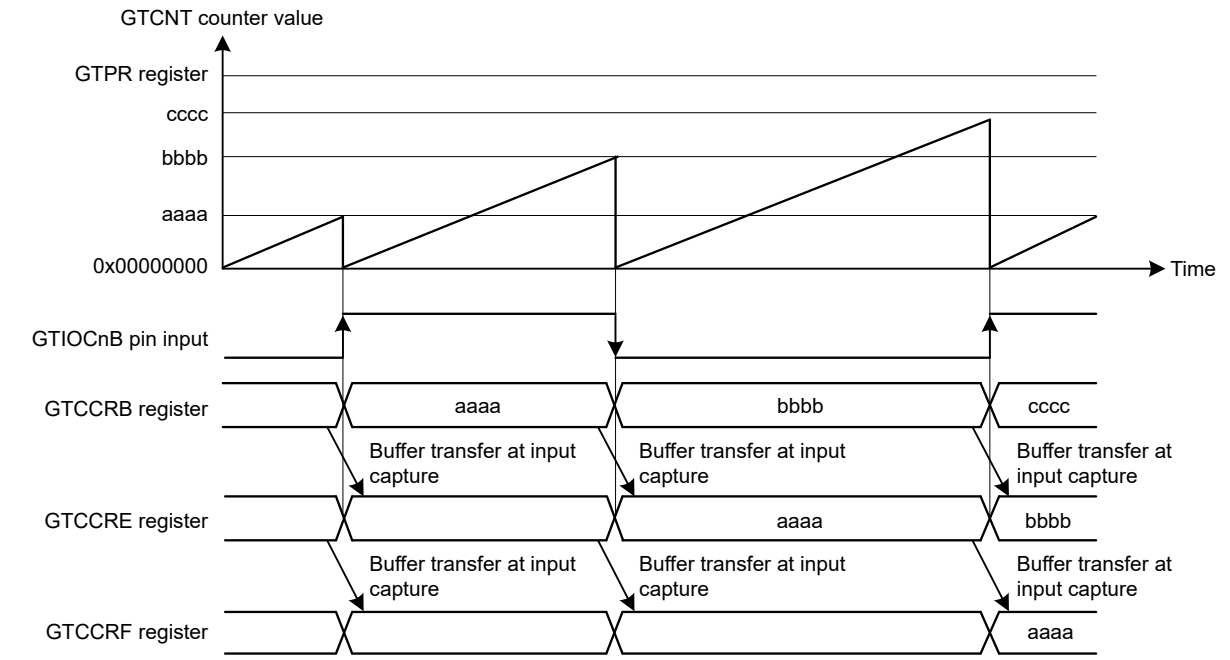
When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 23.26 and Figure 23.27 show examples of GTCCRA and GTCCRB buffer operation and Table 23.21 shows an example for setting GTCCRA and GTCCRB buffer operation.



Note: The base address of registers are the same.

Figure 23.26 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOCnA input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnA input



Note: The base address of registers are the same.

Figure 23.27 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOCnB input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnB input

Table 23.21 Example for setting GTCCRA and GTCCRB buffer operation for input capture

No.	Step Name	Description
1	Set operating mode and counter clear sources	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits and count clear source with the GTCSR register. In Figure 23.26, MD[2:0] = 000b or MD[3:0] = 0000b (saw-wave PWM mode 1) and GTCSR = 0x00000F00, and in Figure 23.27, MD[2:0] = 000b or MD[3:0] = 0000b (saw-wave PWM mode 1) and GTCSR = 0x0000F000.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.26, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode2, set the cycle in the GTPR register. In the saw-wave PWM mode2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select input capture source in the GTICASR register and GTICBSR register. In Figure 23.26, GTICASR = 0x00000F00, and in Figure 23.27, GTICBSR = 0x0000F000. In GPT324 to GPT329 to perform input capture with sources of other channels, select a group that performs inter-channel cooperation by the GTICCR.ICmGRP bit (m = A or B). For the output-side channel of the input capture sources, set the GTICCR register to enables the input capture sources to output to other channels. For input-side channels, set the GTIOmSR.mSOC bit (m = A or B) to 1 to enable input capture with sources of other channels.
7	Set buffer operation	Set buffer operation with the CCRA and CCRB bits in the GTBER register. In Figure 23.26, CCRA[1:0] = 01b, and in Figure 23.27, CCRB[1:0] = 1xb.
8	Start count operation	Set the GTCR.CST bit to 1 to start count operation.

23.3.2.3 Buffer Operation for GTADTRA and GTADTRB Registers

The GTADTBRA register can function as the GTADTRA buffer register and the GTADTDBRA register can function as the GTADTBRA buffer register (double buffer register for the GTADTRA register). Similarly, the GTADTBRB register can function as the GTADTRB buffer register and the GTADTDBRB register can function as the GTADTBRB buffer register (double buffer register for the GTADTRB register).

To set the GTADTRA or GTADTRB register to function as a double buffer, set the GTBER.ADTDA or ADTDB bit to 1. For single buffer operation, set 0. Not to function as buffer, set the GTBER.ADTTA[1:0] or ADTTB[1:0] bits to 00b.

The buffer transfer timing can be set with the ADTTA[1:0] and ADTTB[1:0] bits to an overflow (in up-counting) or an underflow (in down-counting) in saw-wave mode, with ADTTA[1:0] and ADTTB[1:0] bits to 01b for a crest, to 10b for a trough, or to 11b for both crest and trough in triangle-wave mode or complementary PWM mode.

In saw-wave mode, when the ADTTA[1:0] and ADTTB[1:0] bits are set to value other than 00b and in count operation, the buffer transfer, by similar counter clearing sources in section 23.3.2.1. GTPR Register Buffer Operation, is performed in the same way at an overflow (in up-counting) or an underflow (in down-counting).

In complementary PWM mode, the buffer transfer is performed after one GTCLK cycle from GTCCRD register write of slave channel 2.

In saw-wave mode, the buffer transfer of GTADTRm register by counter clearing can be disabled by GTBER2.CCTADm (m = A, B) bit setting.

In saw-wave mode, the buffer transfer of GTADTRm register by its own compare match can be enabled by the GTBER2.CMTADm (m = A, B) bit setting.

Figure 23.28 to Figure 23.32 show examples of buffer operation of the GTADTRA and GTADTRB registers, and Table 23.22 shows an example for setting buffer operation of the GTADTRA and GTADTRB registers.

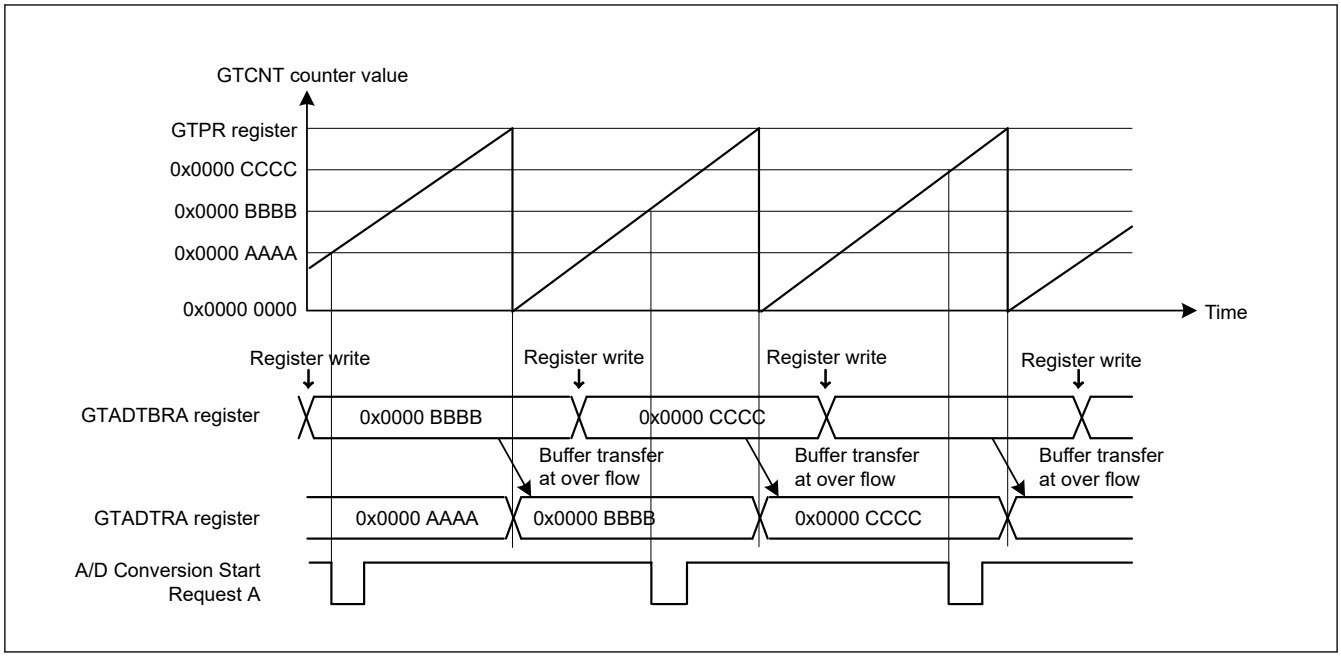


Figure 23.28 Example of Buffer Operation of the GTADTRA and GTADTRB Registers (Saw Waves in Up-Counting, A/D Conversion Start Request Generated by Up-Counting)

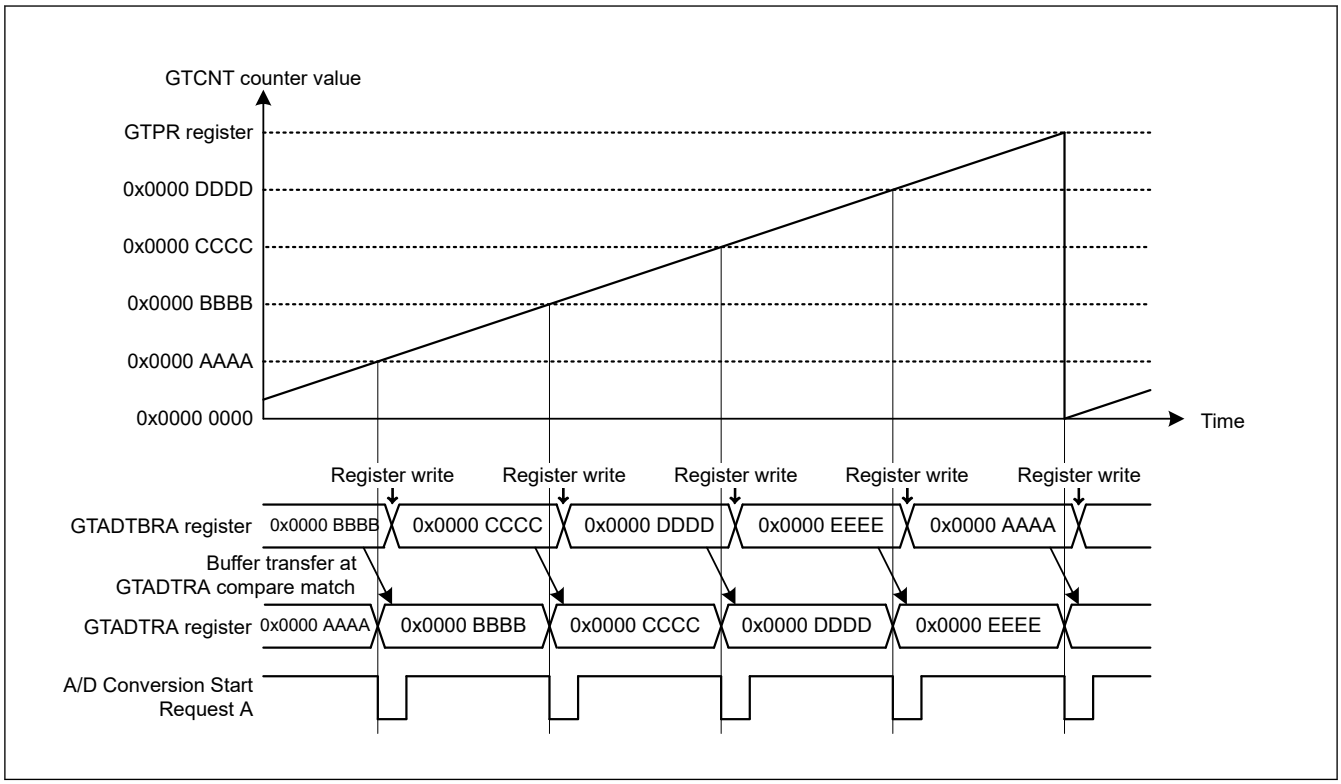


Figure 23.29 Example of Buffer Operation of the GTADTRA and GTADTRB Registers (Saw Waves in Up-Counting, Buffer Transfer at GTADTRA Compare Match, A/D Conversion Start Request Generated by Up-Counting)

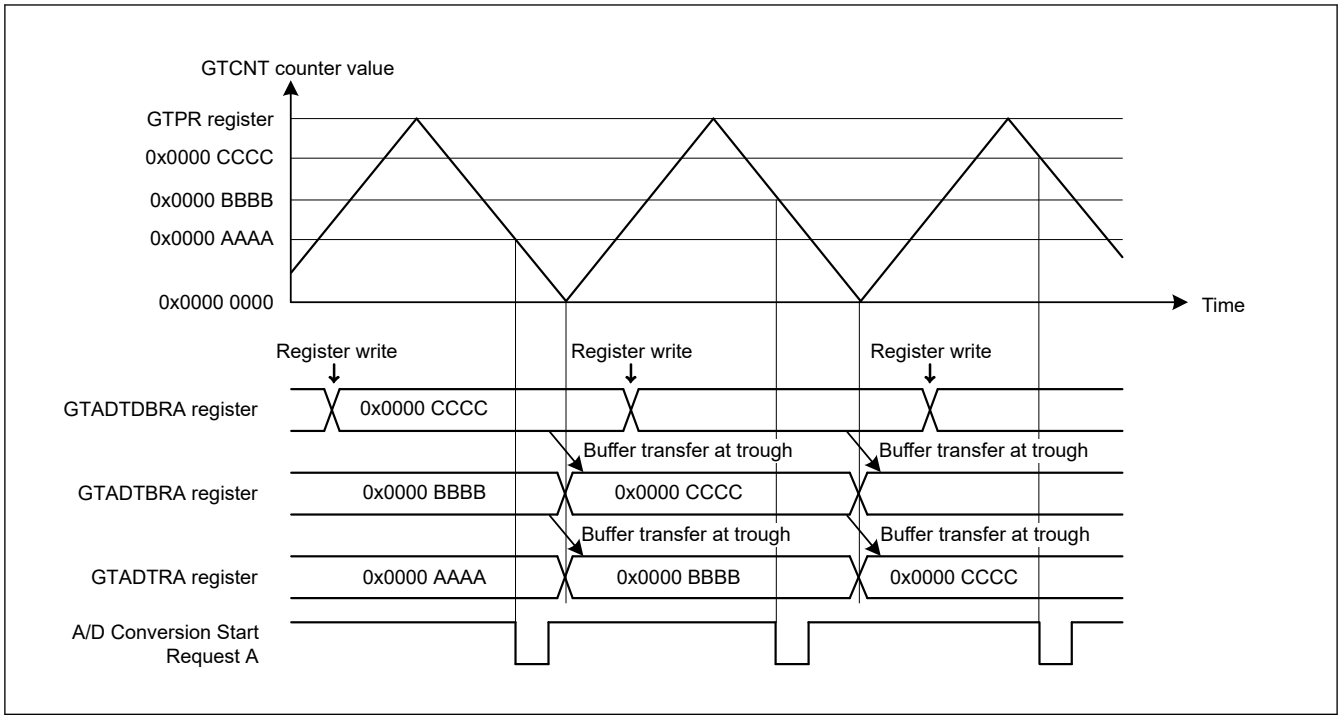


Figure 23.30 **Example of Double Buffer Operation of the GTADTRA and GTADTRB Registers (Triangle Waves, Buffer Transfer at Troughs, A/D Conversion Start Request Generated by Down-Counting)**

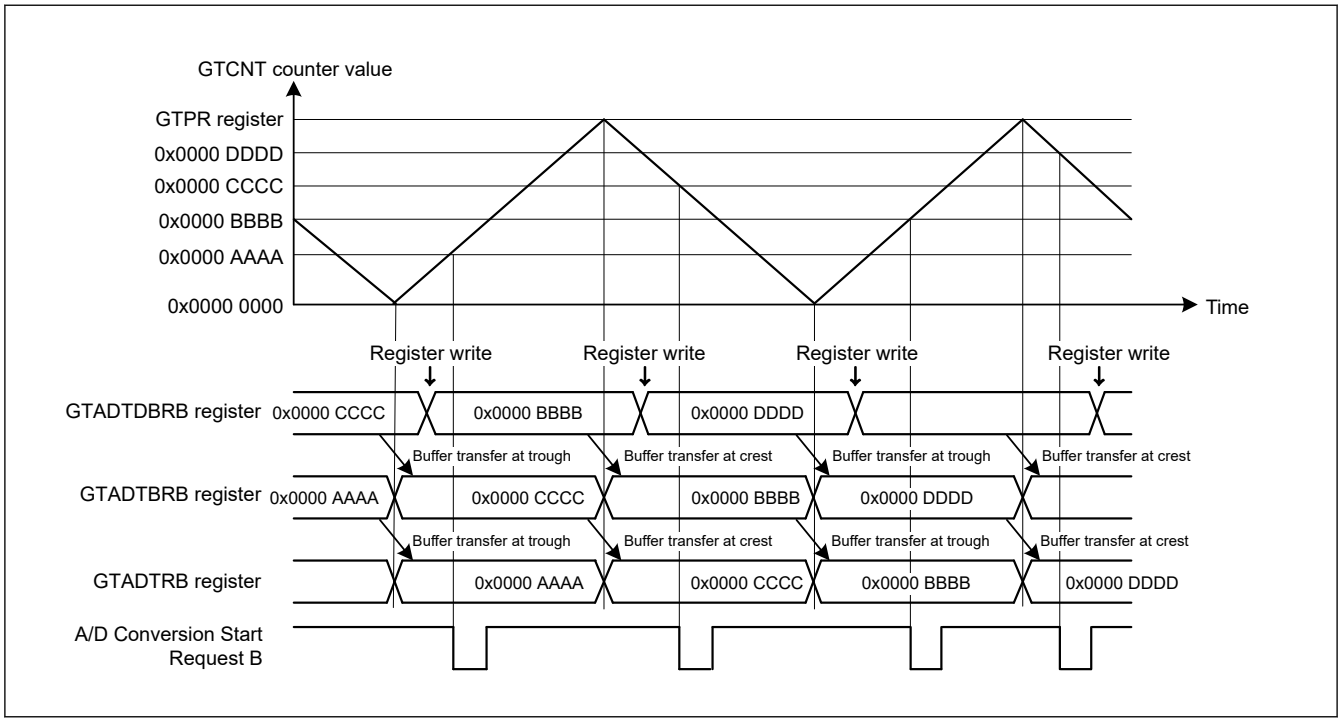


Figure 23.31 **Example of Double Buffer Operation of the GTADTRA and GTADTRB Registers (Triangle Waves, Buffer Transfer at Both Troughs and Crests, A/D Conversion Start Request Generated by Both Up- and Down-Counting)**

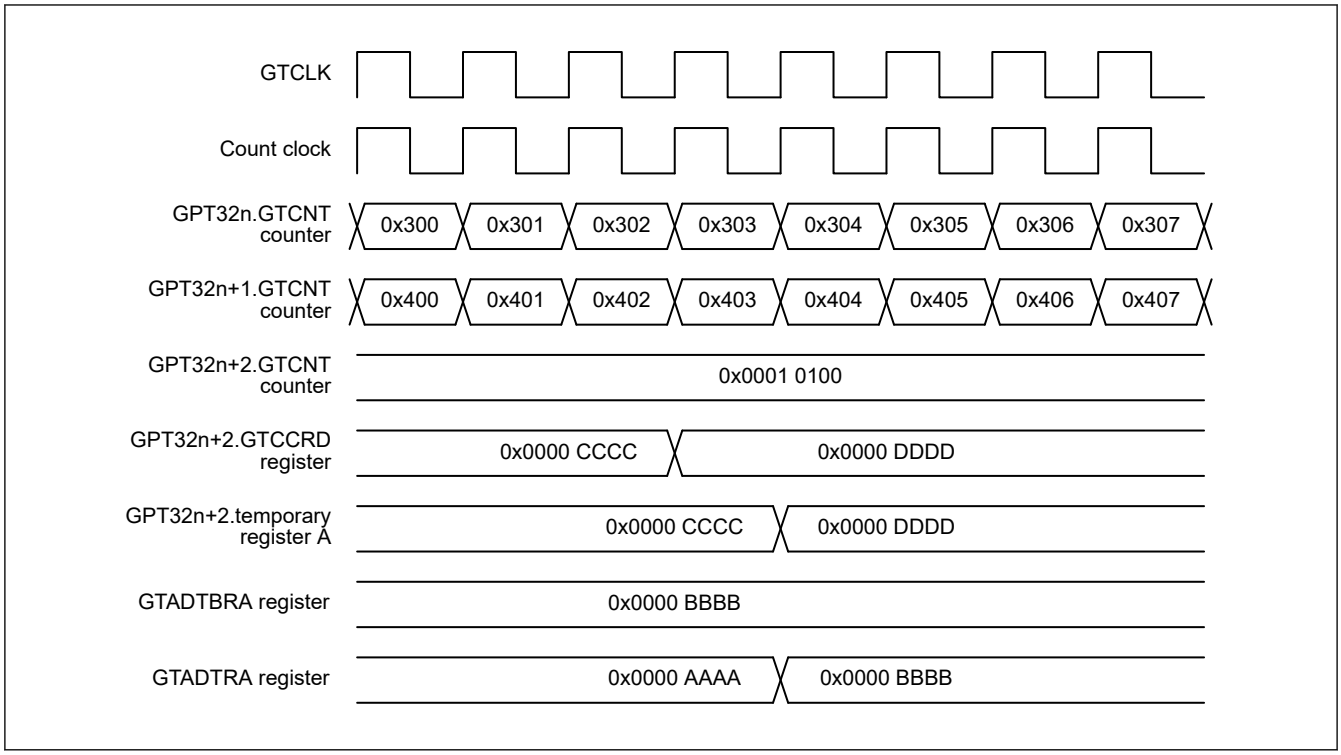


Figure 23.32 Example of Buffer Operation of the GTADTRA and GTADTRB Registers at the GTCCRD Register of Slave Channel 2 Updating in Complementary PWM Mode

Table 23.22 Example for Setting Buffer Operation of the GTADTRA and GTADTRB registers (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. (In Figure 23.28 and Figure 23.29, 000b or 0000b (saw-wave PWM mode 1) is set, in Figure 23.30 and Figure 23.31, 100b, 101b, 110b, 0100b, 0101b, or 0110b (triangle-wave PWM mode) is set.)
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. (In Figure 23.28 and Figure 23.29, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).)
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode 2, set the cycle in the GTPR register. In the saw-wave PWM mode 2, select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with the ADTTA[1:0], ADTTB[1:0], ADTDA, and ADTDB bits in GTBER register. To perform buffer transfer at a compare match of the ADTRAm (m = A, B) register, set the GTBER2.CMTADm bit to 1. (In Figure 23.28, ADTTA[1:0] bits = 01b, 10b, or 11b and ADTDA bit = 0, in Figure 23.29, CMTADA bit = 1, in Figure 23.30, ADTTA[1:0] bits = 10b and ADTDA bit = 1, and in Figure 23.31, ADTTB [1:0] bits = 11b and ADTDB bit = 1.)
7	Set compare match value	Set the A/D conversion start request point in the GTADTRA and GTADTRB registers.
8	Set buffer value	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

Table 23.22 Example for Setting Buffer Operation of the GTADTRA and GTADTRB registers (2 of 2)

No.	Step Name	Description
9	Enable A/D conversion start request	Set to enable A/D conversion start request with the ADTRAUEN, ADTRADEN, ADTRBUEN, and ADTRBDEN bits in the GTINTAD register. (In Figure 23.28 and Figure 23.29, ADTRAUEN bit = 1, in Figure 23.30, ADTRADEN bit = 1, and in Figure 23.31, ADTRBUEN bit = 1 and ADTRBDEN bit = 1.)
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value of each cycle	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

23.3.2.4 Buffer operation for GTIOA and GTIOB

The GTOLBR.GTIOAB[4:0] bits can function as the buffer register of the GTIOR.GTIOA[4:0] bits and the GTOLBR.GTIOBB[4:0] bits can function as the buffer register of the GTIOR.GTIOB[4:0] bits.

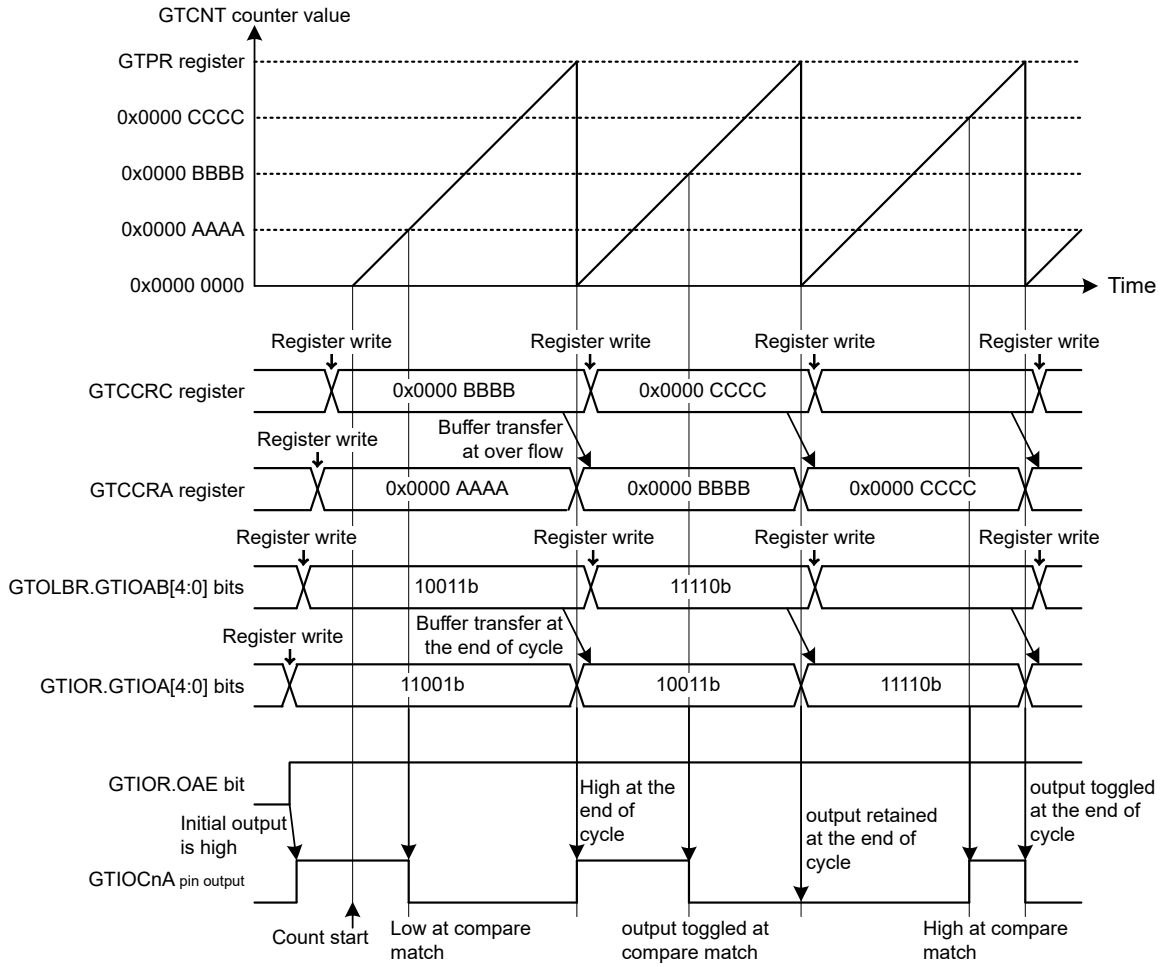
Buffer transfer timing can be set with the GTBER2.OLTTm[1:0] bits (m = A, B). It can be selected from the end of cycle or GTCCR register compare match (in saw-wave mode), from crest, trough, or both crest and trough (in triangle-wave mode and complementary PWM mode). In the case that the GTBER2.OLTTm[1:0] bits are 00b, buffer transfer is not performed.

In complementary PWM mode, the setting to convert GTIOA and GTIOB by buffer transfer during the dead time of complementary PWM is prohibited.

Therefore, when changing GTIOA and GTIOB by buffer transfer, it is necessary to set the crest and trough timings not to overlap with the dead time and change GTOLBR.GTIOAB and GTOLBR.GTIOBB.

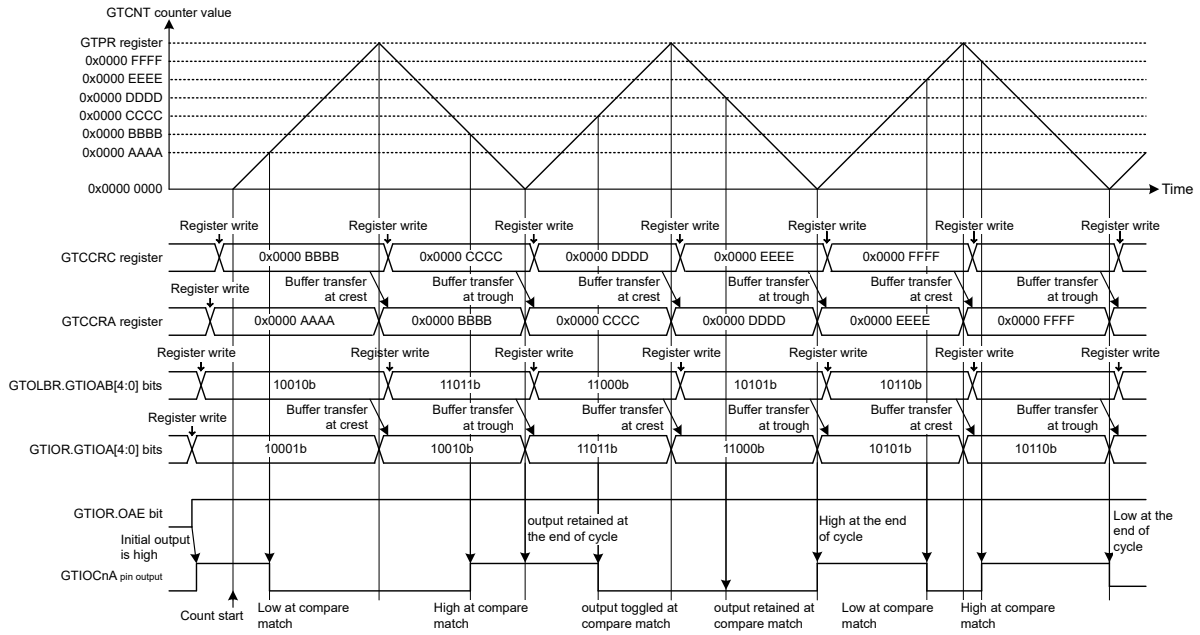
When the buffer transfer timing is crest, set the GTCCRm (m = A, C, E) register to satisfy GTCCRm < GTPR. And when the buffer transfer timing is trough, set the GTCCRm register to satisfy GTDVU < GTCCRm.

Figure 23.33 to Figure 23.35 show examples of buffer operation of the GTIOR.GTIOA[4:0] and GTIOR.GTIOB[4:0] bits. Table 23.23 shows an example for setting buffer operation of the GTIOR.GTIOA[4:0] and GTIOR.GTIOB[4:0] bits.



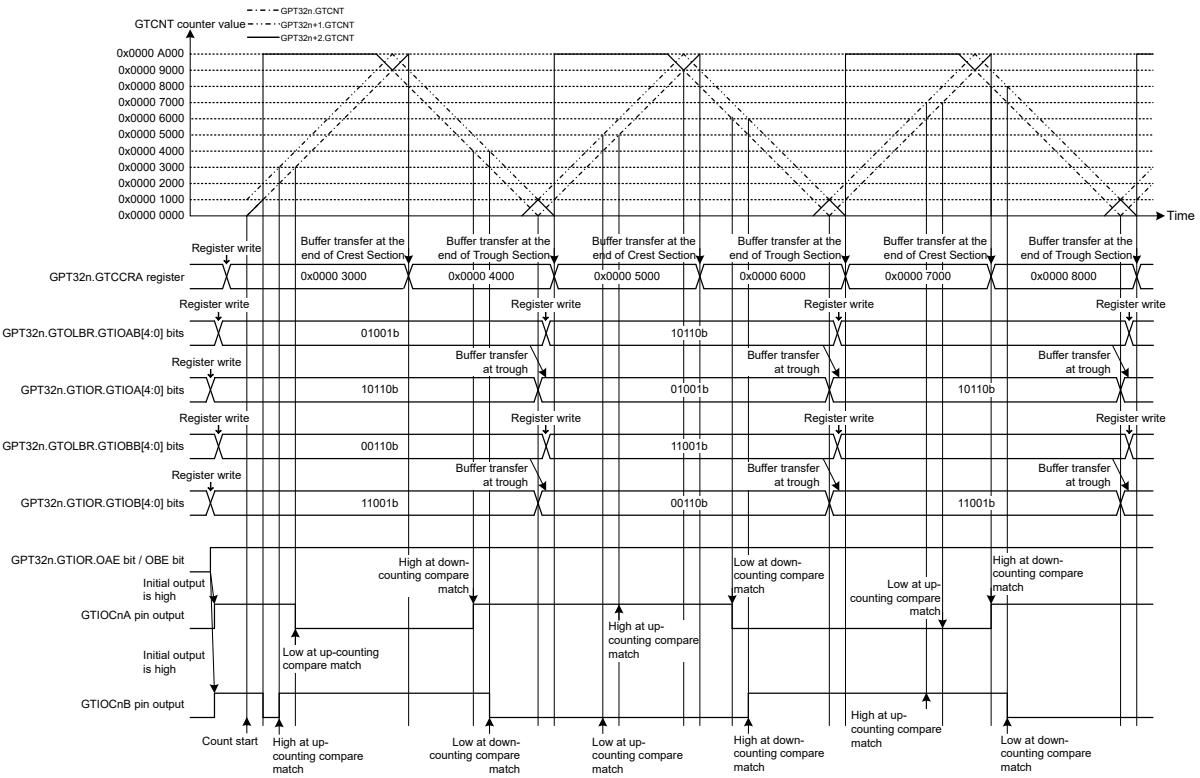
Note: Initial output is synchronized to the count clock.

Figure 23.33 Example of Buffer Operation of the GTIOA and GTIOB Bits (Up-Counting in Saw-Wave PWM Mode 1, Buffer Transfer at the End of Cycle)



Note: Initial output is synchronized to the count clock.

Figure 23.34 Example of Buffer Operation of the GTIOA and GTIOB Bits (Triangle-Wave PWM Mode 2, Buffer Transfer at Crests and Troughs)



Note: Initial output is synchronized to the count clock.

Figure 23.35 Example of Buffer Operation of the GTIOA and GTIOB Bits (Complementary PWM Mode 3, Buffer Transfer at Troughs)

Table 23.23 Example for Setting Buffer Operation of the GTIOA and GTIOB

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0]. (In Figure 23.33, 0000b (saw-wave PWM mode 1) is set, in Figure 23.34, 0101b (triangle-wave PWM mode 2) is set, in Figure 23.35, 1110b (complementary PWM mode 3) is set.)
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. (In Figure 23.33, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).)
3	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits.
4	Set cycle	Other than the saw-wave PWM mode 2, Set the cycle in GTPR. In the saw-wave PWM mode 2, Select the counter clear source compare match register GTCCRx (x = A to F) by GTCSR.CSCMSC[2:0] bits and set the cycle in that register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. (In Figure 23.33, GTIOA[4:0] = 11001b, in Figure 23.34, GTIOA[4:0] = 10001b, in Figure 23.35, GTIOA[4:0] = 10110b and GTIOB[4:0] = 11001b.)
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer operation	Set buffer operation with OLTTm[1:0] bits in GTBER2 register. (In Figure 23.33, 01b is set in OLTTA[1:0], in Figure 23.34, 11b is set in OLTTA[1:0], in Figure 23.35, 10b is set in OLTTA[1:0] and 10b is set in OLTTB[1:0].)
9	Set buffer value	For buffer operation, set the GTIOCnm pin function in one cycle after the current cycle (in saw-wave mode and in triangle-wave/complementary PWM mode with buffer transfer at crest or trough) or half cycle after the current cycle (in triangle-wave/complementary PWM mode with buffer transfer at crest and trough) in the GTOLBR register.
10	Start count operation	Set GTCR.CST to 1 to start count operation.
11	Set buffer value of each cycle	For buffer operation, set the GTIOCnm pin function in one cycle after the current cycle (in saw-wave mode and in triangle-wave/complementary PWM mode with buffer transfer at crest or trough) or half cycle after the current cycle (in triangle-wave/complementary PWM mode with buffer transfer at crest and trough) in the GTOLBR register.

Note: n = 4 to 9
m = A, B

23.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA or GTIOCnB pin (n = 0 to 13) by a compare match between the GTCNT counter and GTCCRA or GTCCRB.

By setting GTDTCR, GTDVU, and GTDVD, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

In complementary PWM mode, it is possible to output PWM waveforms (positive phase, negative phase) with dead time that guarantees the linearity of the PWM output pulse width near 0% and 100% duty.

In saw-wave mode other than saw-wave PWM mode 2, or triangle-wave mode, or the master channel of complementary PWM mode, the signal synchronized with the PWM cycle can be output from the GTCPPOn output terminal by setting the GTIOR.PSYE bit to 1. The GTCPPOn output is toggled at the end of cycle in saw-wave mode or at the timing of crest / trough / GTCNT counter clearing in triangle-wave mode or complementary PWM mode. The initial output of GTCPPOn is low, and it becomes high when the count starts.

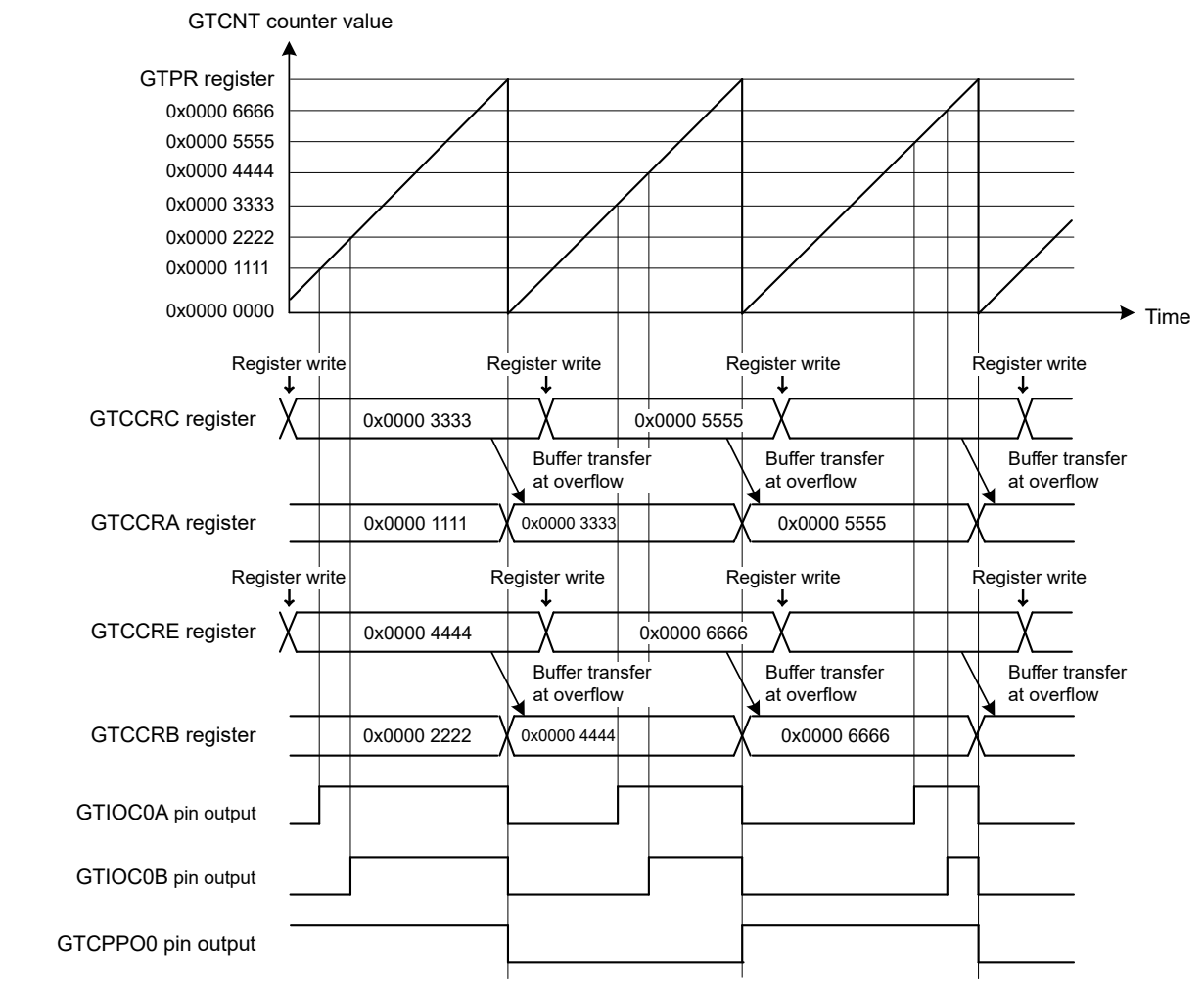
23.3.3.1 Saw-Wave PWM Mode 1

In saw-wave PWM mode 1, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 13) when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

When 0 is set in the GTIOR.OxEOCD (x = A, B) bit and the timing of the end of cycle and the timing of GTCCRx register compare match are the same time, the output pin performs along the PWM output setting for the end of cycle set by the GTIOR.GTIOx[3:2] bit.

When 1 is set in the GTIOR.OxEOCD bit, GTIOCnx output is retained.

Figure 23.36 shows an example of saw-wave PWM mode 1 operation, and Table 23.24 shows an example for setting saw-wave PWM mode 1.



Note: The base address of registers are the same.

Figure 23.36 Example of saw-wave PWM mode 1 operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, low output at cycle end, and GTIOR.PSYE = 1

Table 23.24 Example for setting saw-wave PWM mode 1 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.36, 000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.36, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.36, GTIOA[4:0] = 00110b and GTIOB[4:0] = 00110b.
7	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.

Table 23.24 Example for setting saw-wave PWM mode 1 (2 of 2)

No.	Step Name	Description
8	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
9	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 23.36, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
10	Set compare match value*1	Set the GTIOCnA pin transition in the GTCCRA register and the GTIOCnB pin transition in the GTCCRB register.
11	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.
12	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
13	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 13
m: A, B

Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

23.3.3.2 Saw-Wave PWM Mode 2

The saw-wave PWM mode 2 is a mode in which the GTCNT counter is operated as a saw wave by up-counting without using the GTPR register, and the PWM waveform is output by the compare match of the GTCCRA and GTCCRB registers. The pin output level can be selected from low output, high output, or toggle output separately for a compare match according to the GTIOR register setting.

The GTIOCnA pin is used as an output pin. Use the GTIOR.GTIOB[1:0] bits for setting the GTIOCnA pin output at a compare match of the GTCCRB register.

When a counter clear occurs due to the GTCNT counter clearing source selected in the GTCSR register, this is handled at the end of cycle and PWM output operation at the end of the cycle selected with the GTIOR.GTIOA[3:2] bits is performed. If a counter clear (at the end of cycle) conflicts with a PWM output change due to a GTCCRx (x = A, B) register compare match, PWM output operation is performed at the end of cycle (in the case of the GTIOR.OxEOCD bit = 0) or the PWM output is retained (in the case of GTIOR.OxEOCD bit = 1).

Figure 23.37 to Figure 23.39 shows an example of saw-wave PWM mode 2 operation. Table 23.25 shows an example for setting saw-wave PWM mode 2.

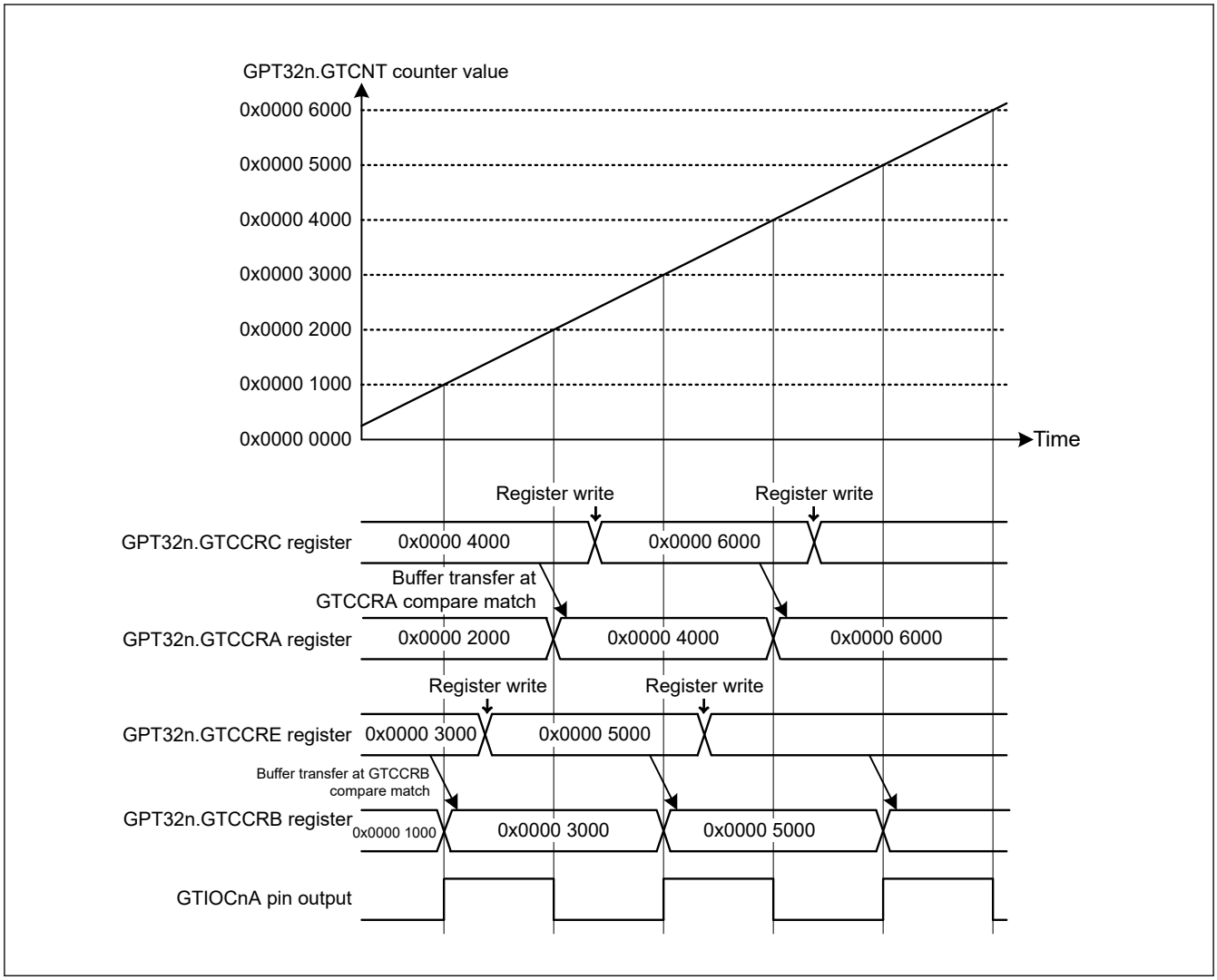


Figure 23.37 Example of Saw-Wave PWM Mode 2 Operation (Low Output at GTCCRA Register Compare Match, High Output at GTCCRB Register Compare Match, Single Buffer Operation, No Clear Setting) (n = 4 to 9)

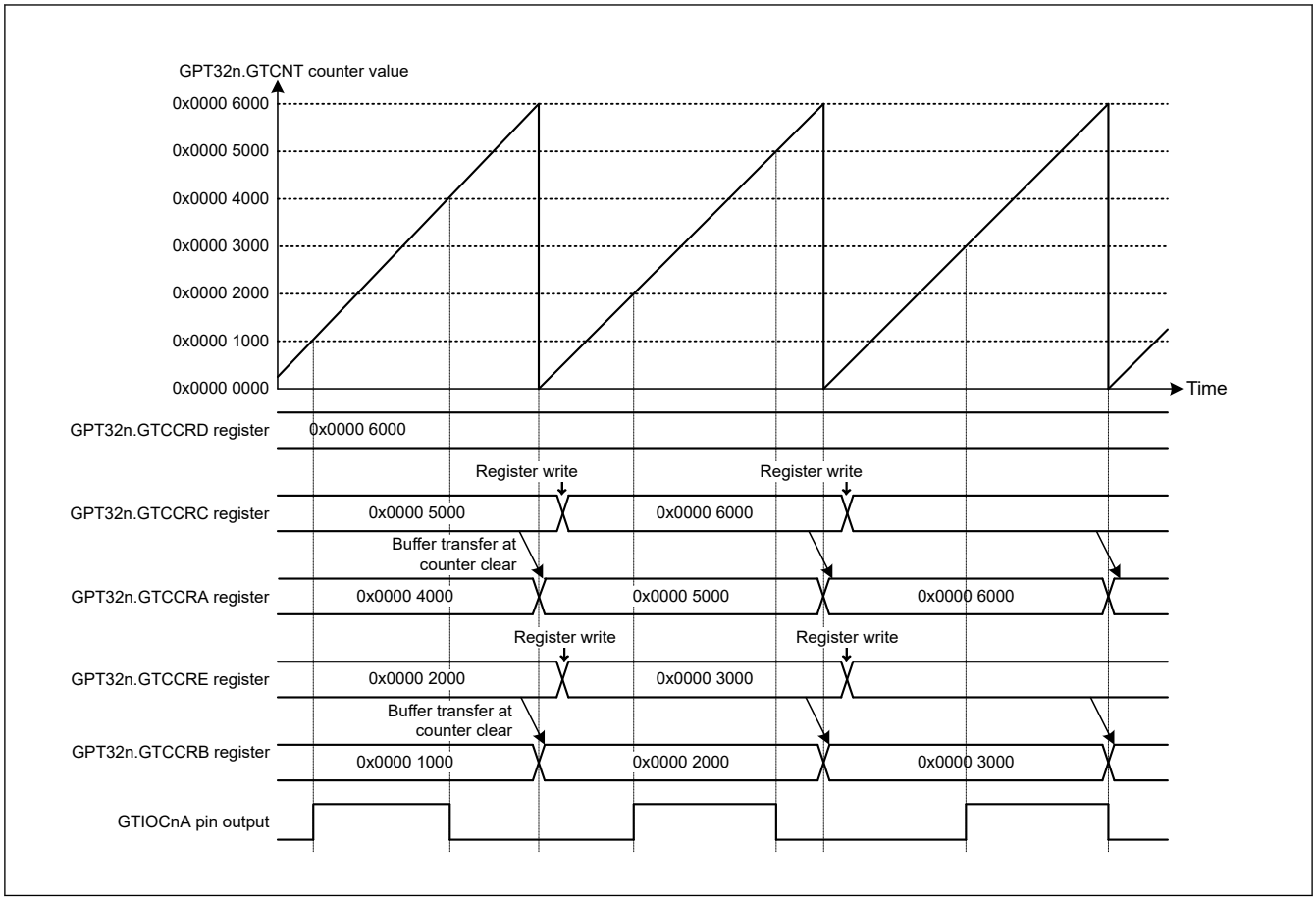


Figure 23.38 Example of Saw-Wave PWM Mode 2 Operation (Low Output at GTCCRA Register Compare Match, High Output at GTCCRB Register Compare Match, Low Output at the End of Cycle, Single Buffer Operation, Cleared at GTCCRD Register Compare Match, GTIOR.OAEOCD Bit = 0) (n = 4 to 9)

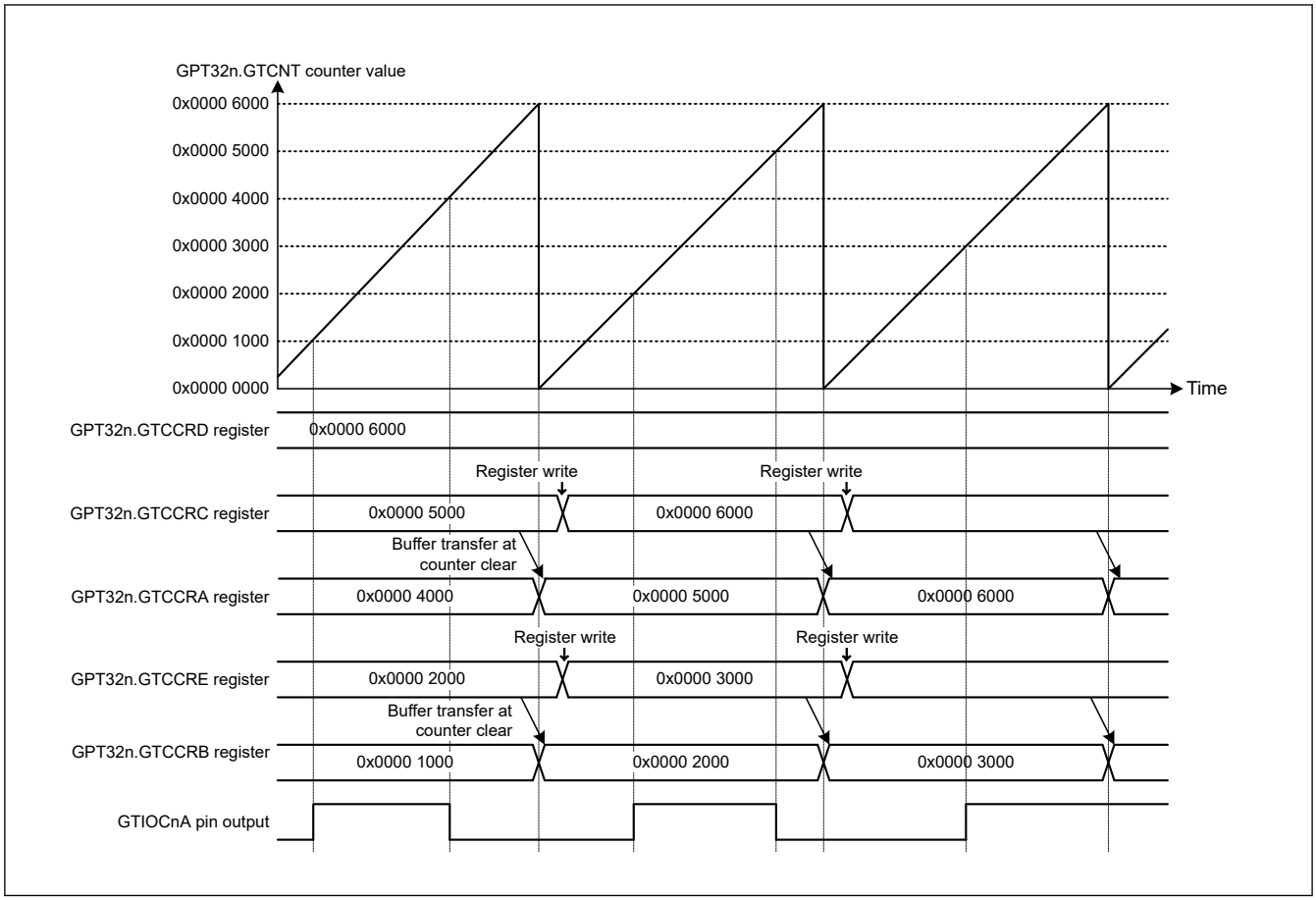


Figure 23.39 Example of Saw-Wave PWM Mode 2 Operation (Low Output at GTCCRA Register Compare Match, High Output at GTCCRB Register Compare Match, Low Output at the End of Cycle, Single Buffer Operation, Cleared at GTCCRD Register Compare Match, GTIOR.OAEOCD Bit =1) (n = 4 to 9)

Table 23.25 Example for Setting Saw-wave PWM mode 2

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0]. (In Figure 23.37 to Figure 23.39, 0010b (saw-wave PWM mode 2) is set.)
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Set GTIOCnA pin function	Set the GTIOCnA pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. (In Figure 23.37 to Figure 23.39, GTIOA[4:0] = 00001b and GTIOB[1:0] = 10b.)
5	Enable GTIOCnA pin output*1	Set to enable the GTIOCnA pin output with OAE in GTIOR.
6	Set buffer operation	Set buffer operation with CCRA[1:0] and CCRB[1:0] bits in GTBER (In Figure 23.37 to Figure 23.39, CCRA[1:0] = 01b and CCRB[1:0] = 01b.)
7	Set compare match value*1	Set the GTIOCnA pin changing point in GTCCRA and GTCCRB.
8	Set buffer value	For buffer operation, set the GTCCRA register value and the GTCCRB register value which used in one cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTCCRA register value and the GTCCRB register value which used in two cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.
9	Start count operation	Set GTCR.CST to 1 to start count operation.
10	Set buffer value of each cycle	For buffer operation, set the GTCCRA register value and the GTCCRB register value which used in one cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTCCRA register value and the GTCCRB register value which used in two cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

Note: n: 4 to 9
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnA pin output enable and setting for a compare match value.

23.3.3.3 Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR, the GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 13) at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

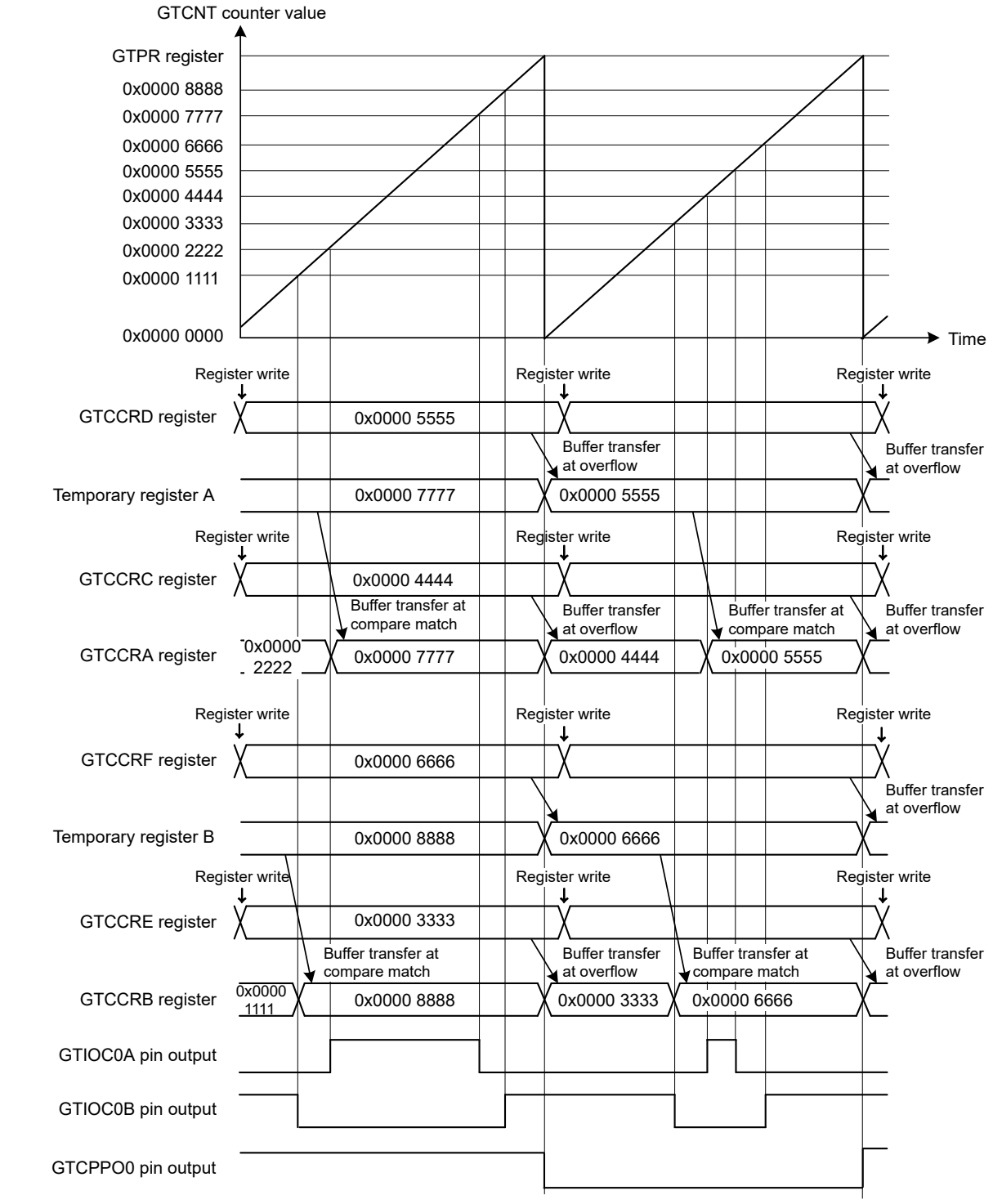
Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

When the GTBER.DBRTECm (m = A, B) bit is set to 1, transfer from an intermediate buffer to the GTCCRm register is repeated on a cyclic basis with using the temporary register x (x = C, E) and temporary register m which operate as intermediate buffers for the GTCCRx and GTCCRm registers, respectively, even while buffer transfer is disabled (repeated double buffer operation function during disabling of buffer transfer). For details, see section 23.8.2.2. Repeated Double-Buffered Operation When Disabling GTCCR Buffer Transfer.

Figure 23.40 shows an example of saw-wave one-shot pulse mode operation, and Table 23.26 shows an example for setting saw-wave one-shot pulse mode.



Note: The base address of registers are the same.

Figure 23.40 Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, output retained at cycle end, and GTIOR.PSYE = 1

Table 23.26 Example setting for saw-wave one-shot pulse mode

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.40, 001b (saw-wave one-shot pulse mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.40, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.40, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
8	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
9	Set compare match value*1	Set the GTIOCnA pin transition immediately after the count start in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
10	Set forcible buffer transfer*1	Set the GTBER.CCRSWT bit to 1 to transfer buffer register data forcibly.
11	Set buffer value	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
12	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
13	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.

Note: n: 0 to 13
m: A, B

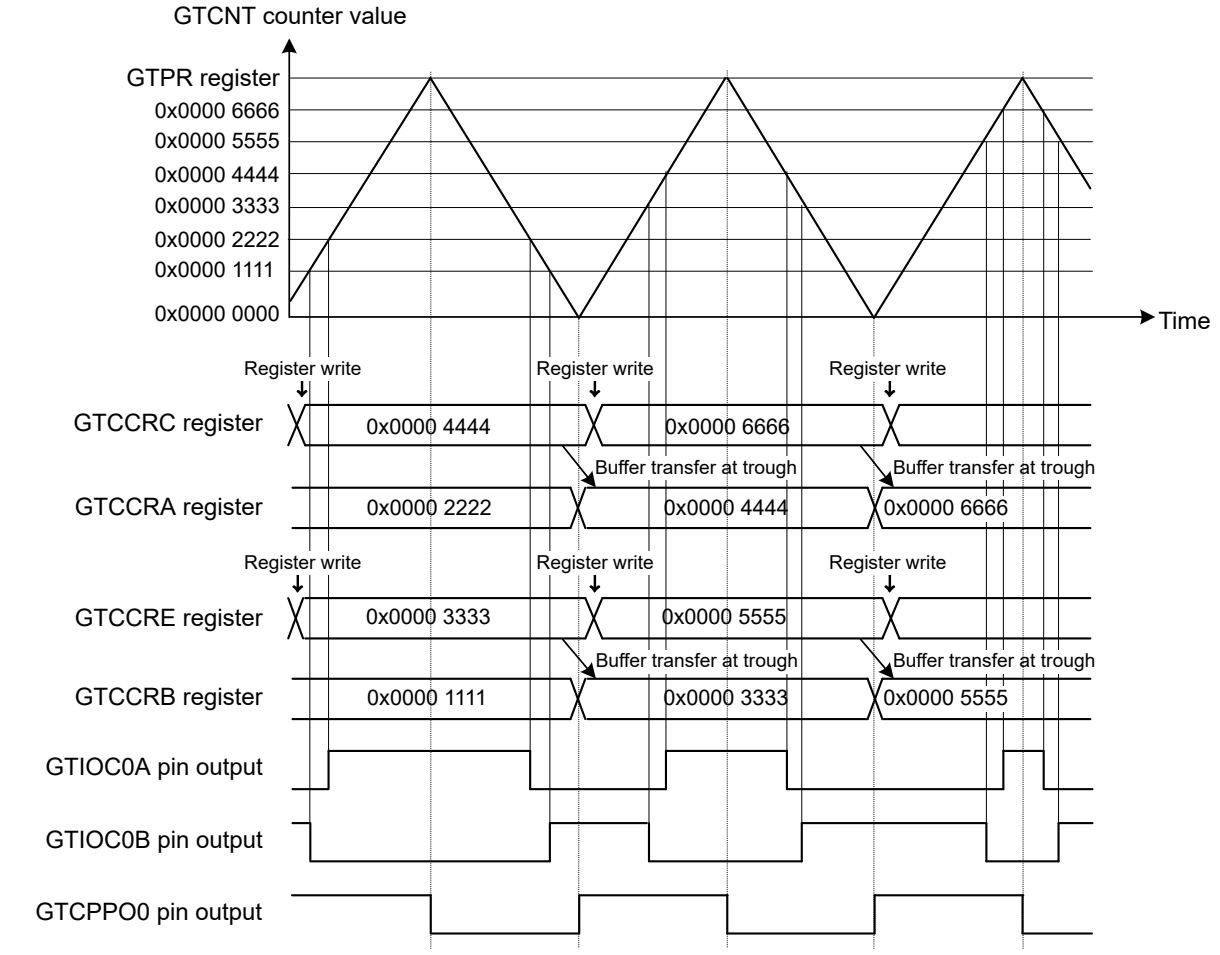
Note 1. When using PWM Delay Generation circuit, change the order of Enable GTIOCnm pin output and Set compare match value + Set forcible buffer transfer.

23.3.3.4 Triangle-Wave PWM Mode 1 (32-Bit Transfer at Trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 13) when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.41 shows an example of a triangle-wave PWM mode 1 operation, and Table 23.27 shows an example for setting a triangle-wave PWM mode 1.



Note: The base address of registers are the same.

Figure 23.41 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB register compare match, output retained at cycle end, and GTIOR.PSYE = 1

Table 23.27 Example setting for triangle-wave PWM mode 1 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.41, 100b (triangle-wave PWM mode 1) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.41, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 23.41, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
9	Set compare match value*1	Set the GTIOCnA and GTIOCnB pins transitions in the GTCCRA and GTCCRB registers, respectively.

Table 23.27 Example setting for triangle-wave PWM mode 1 (2 of 2)

No.	Step Name	Description
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle in the GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 13
m: A, B

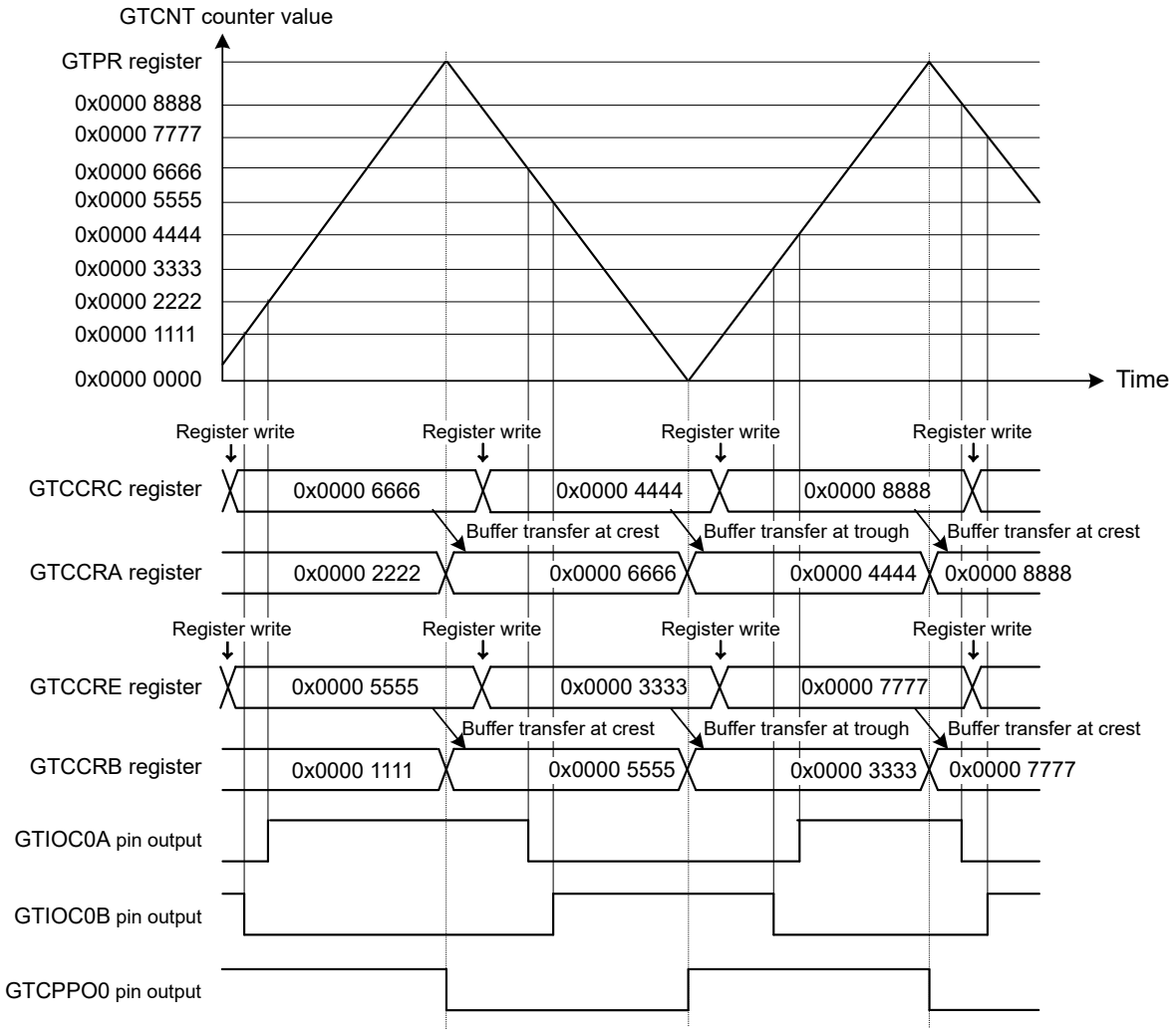
Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

23.3.3.5 Triangle-Wave PWM Mode 2 (32-Bit Transfer at Crest and Trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 13) when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.42 shows an example of triangle-wave PWM mode 2 operation, and Table 23.28 shows an example for setting triangle-wave PWM mode 2.



Note: The base address of registers are the same.

Figure 23.42 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, output retained at cycle end, and GTIOR.PSYE = 1

Table 23.28 Example for setting triangle-wave PWM mode 2 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.42, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.42, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set buffer operation	Set buffer operation with the CCRA[1:0] and CCRB[1:0] bits in the GTBER register. In Figure 23.42, CCRA[1:0] = 01b and CCRB[1:0] = 01b.

Table 23.28 Example for setting triangle-wave PWM mode 2 (2 of 2)

No.	Step Name	Description
9	Set compare match value*1	Set the GTIOCnA and GTIOCnB pins transitions in the GTCCRA and GTCCRB registers, respectively.
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in half cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in the GTCCRD and GTCCRF registers, respectively.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each half cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in half cycle after the current cycle in the GTCCRC and GTCCRE registers, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle in GTCCRD and GTCCRF registers, respectively.

Note: n: 0 to 13
m: A, B

Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

23.3.3.6 Triangle-Wave PWM Mode 3 (64-Bit Transfer at Trough)

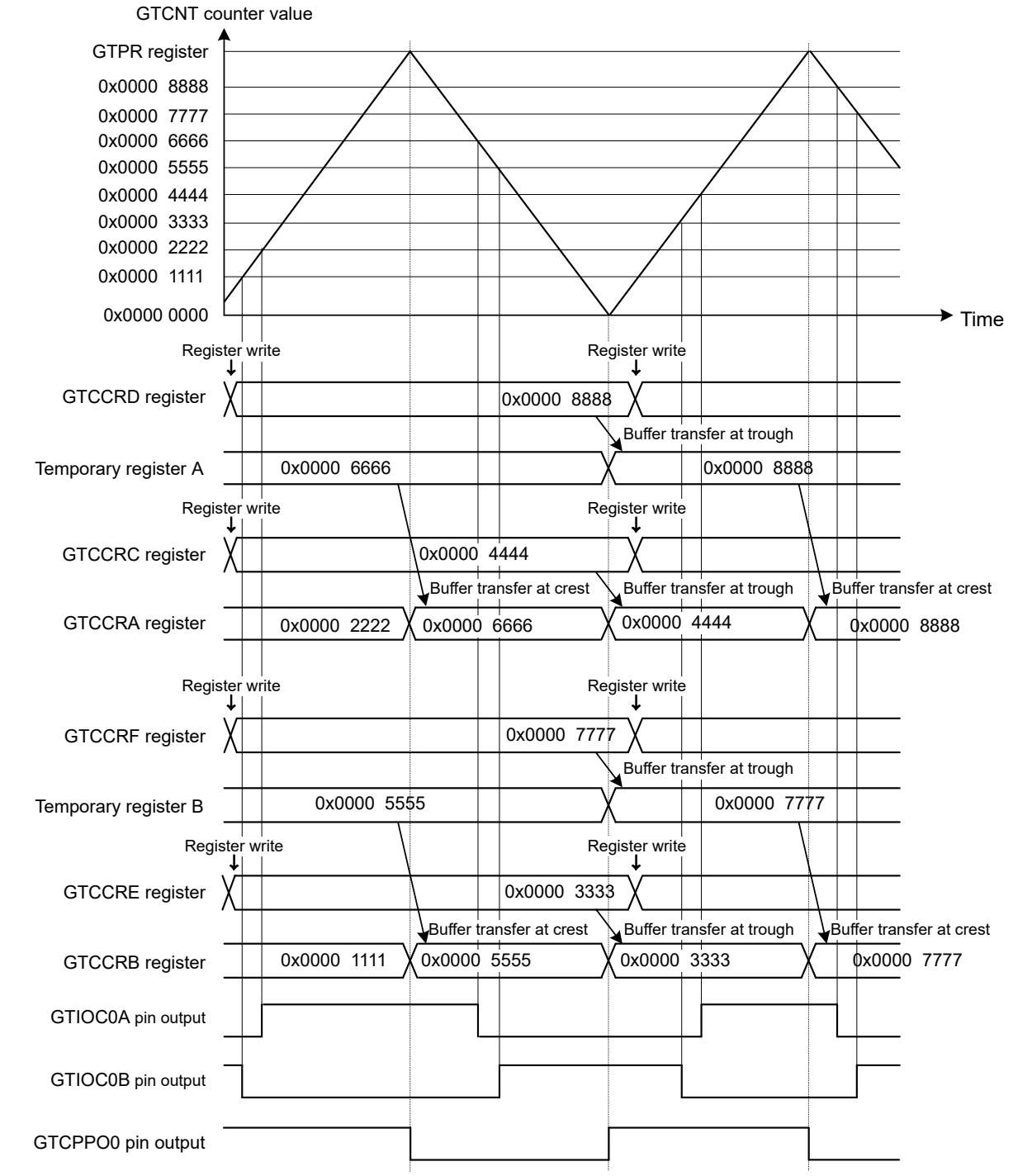
The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin (n = 0 to 13) at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from the following:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.43 shows an example of triangle-wave PWM mode 3 operation, and Table 23.29 shows an example for setting triangle-wave PWM mode 3.



Note: The base address of registers are the same.

Figure 23.43 Example of triangle-wave PWM mode 3 operation with low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/GTCCRB compare match, output retained at cycle end, and GTIOR.PSYE = 1

Table 23.29 Example setting for triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.43, 110b (triangle-wave PWM mode 3) is set.

Table 23.29 Example setting for triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with the GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register. In Figure 23.43, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTCPPOn pin output	Set to enable/disable the GTCPPOn pin output with the PSYE bit in the GTIOR register.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with the OAE and OBE bits in the GTIOR register.
8	Set compare match value*1	Set the GTIOCnA pin transition immediately after the count start in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
9	Set forcible buffer transfer*1	Set the GTBER.CCRSWT bit to 1 to transfer buffer register data forcibly.
10	Set buffer value	Set the GTIOCnA pin transition in 1 cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.
11	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
12	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in the GTCCRC and GTCCRD registers and the GTIOCnB pin transition in the GTCCRE and GTCCRF registers.

Note: n: 0 to 13
m: A, B

Note 1. When using PWM Delay Generation circuit, change the order of Enable GTIOCnm pin output and Set compare match value + Set forcible buffer transfer.

23.3.3.7 Complementary PWM mode 1, 2, 3

In complementary PWM mode, a three-phase PWM waveform with dead time that ensures the linearity in the vicinity of duty 0% and 100% can be output using the GTCNT counter of consecutive three channels. There are four modes depending on differences in buffer operation: (1) complementary PWM mode 1 (transfer at crests), (2) complementary PWM mode 2 (transfer at troughs), (3) complementary PWM mode 3 (transfer at crests and troughs), and (4) complementary PWM mode 4 (immediate transfer).

Figure 23.44 shows the block diagram in complementary PWM modes 1 to 3.

Among consecutive three channels, the lowest channel is referred to as master channel, and the adjacent upper two channels are referred to as slave channel 1 (lower) and slave channel 2 (upper).

The GTCNT counter of each channel performs individual count operation under the cycle operation by the master channel. In each channel, compare match with the GTCCRA register is performed selecting one of the three GTCNT counters in each operation section, and a positive-phase waveform and a negative-phase waveform are output from the GTIOCn+iA pin (i = 0, 1, 2) and the GTIOCn+iB pin respectively with a non-overlapping section of the dead time value set in the GTDVU register of the master channel.

The GTCCRA register performs buffer operation by the GTCCRC register, temporary register A, and GTCCRD register. In complementary PMW mode 3, setting the GTBER2.CP3DB bit to 1 also enables buffer operation of the GTCCRA register by the GTCCRE register, temporary register B, and GTCCRF register, allowing double buffer operation.

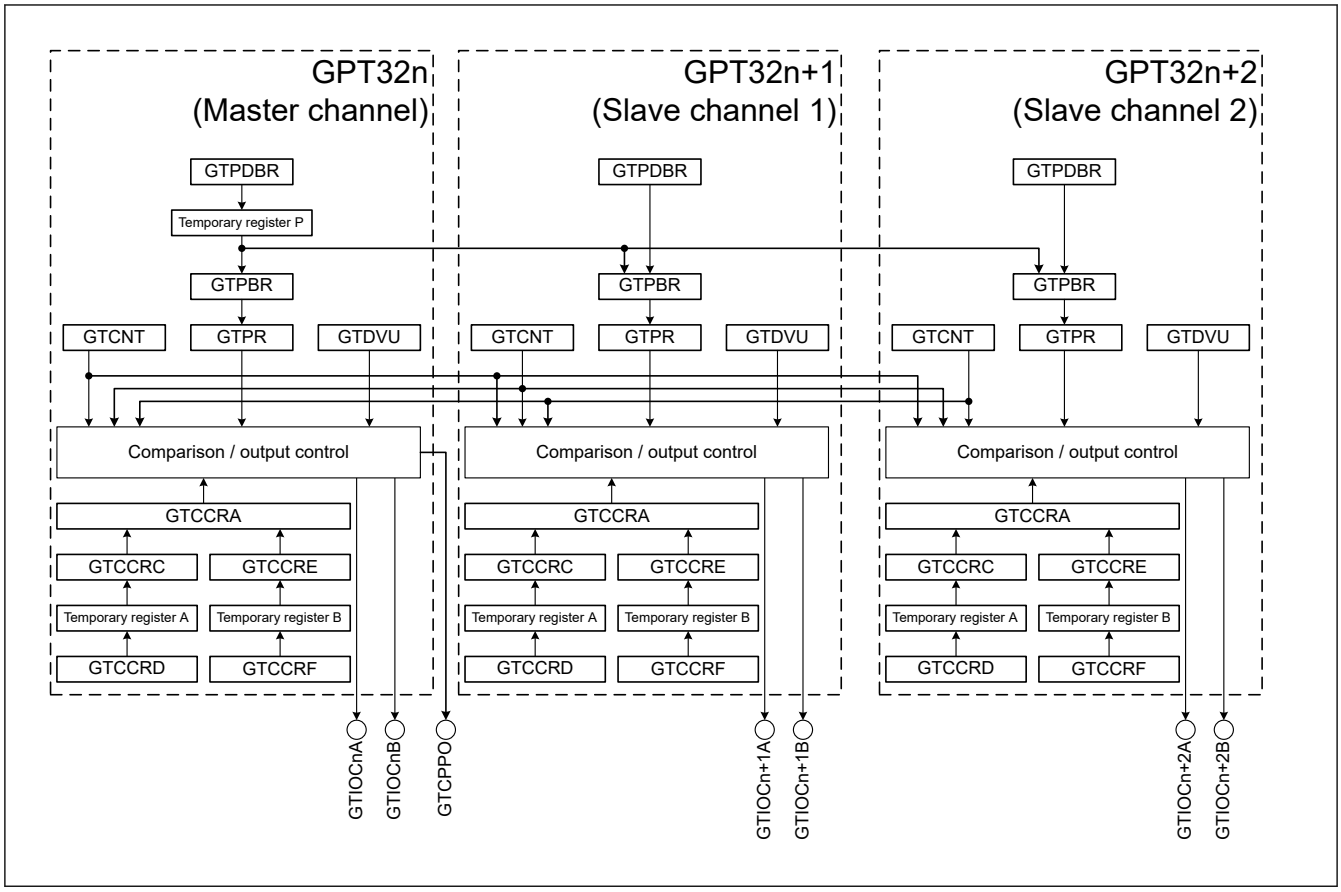


Figure 23.44 Block Diagram in Complementary PWM Mode 1, 2, 3 (n = 4, 7)

The GPT32n.GTCNT counter performs count operation for triangle waves using the GPT32n.GTPR register as a cycle register. A section where the GPT32n.GTCNT counter value is not larger than the dead time value is referred to as trough section.

The GPT32n+1.GTCNT counter performs count operation with the value (GPT32n.GTCNT counter value + dead time value set in the GPT32n.GTDVU register). A section where the GPT32n+1.GTCNT counter value is larger than the GPT32n.GTPR register value is referred to as crest section.

Crest section and trough section are classified into up-counting crest section, down-counting crest section, up-counting trough section, and down-counting trough section according to counting direction. A section between trough section and crest section is referred to as up-counting middle section or down-counting middle section according to counting direction. A section equivalent to the up-counting trough section after starting count operation is referred to as initial output section where operation differs partially from other up-counting trough sections.

The GPT32n+2.GTCNT counter functions as a counter to ensure the linearity in the vicinity of duty 0% and 100%. In a crest section, this counter performs count operation for a triangle wave (up-counting after down-counting) with the value (GPT32n.GTPR register value + dead time value) as an initial value and the GPT32n.GTPR register value as a trough. This counter is cleared to 0 at the end of the crest section, and then stops counting until the next trough section. In a trough section, this counter performs count operation for a triangle wave with an initial value of 0 and dead time value as a crest. This counter becomes the value (GPT32n.GTPR register value + dead time value) at the end of the trough section, and then stops counting until the next crest section. In the initial output section, however, this counter counts up with an initial value of 0 until the dead time value, and then becomes the value (GPT32n.GTPR register value + dead time value).

If the counter stops and then restarts in complementary PWM mode, the counter of each channel returns to the initial value after starting count operation, and then starts counting from the initial output section.

Table 23.30 and Table 23.31 shows count operation (counting direction/counting range) in each section. In these tables, registers with no channel identification indicate that the same value is stored in them of the master channel, slave channel 1, and slave channel 2.

Table 23.30 Count Operation in Complementary PWM Mode

Counter	Initial Value	Initial Output Section (After Start)	Up-Counting Middle Section	Up-Counting Crest Section	Down-Counting Crest Section
GPT32n.GTCNT	0	Up-counting 0 to GTDVU	Up-counting GTDVU+1 to GTPR-GTDVU	Up-counting GTPR-GTDVU+1 to GTPR	Down-counting GTPR-1 to GTPR-GTDVU
GPT32n+1.GTCNT	GTDVU	Up-counting GTDVU to GTDVU×2	Up-counting GTDVU×2+1 to GTPR	Up-counting GTPR+1 to GTPR+GTDVU	Down-counting GTPR+GTDVU-1 to GTPR
GPT32n+2.GTCNT	0	Up-counting 0 to GTDVU	Stop GTPR+GTDVU	Down-counting GTPR+GTDVU-1 to GTPR	Up-counting GTPR+1 to GTPR+GTDVU

Table 23.31 Count Operation in Complementary PWM Mode

Counter	Down-Counting Middle Section	Down-Counting Trough Section	Up-Counting Trough Section
GPT32n.GTCNT	Down-counting GTPR-GTDVU-1 to GTDVU	Down-counting GTDVU-1 to 0	Up-counting 1 to GTDVU
GPT32n+1.GTCNT	Down-counting GTPR-1 to GTDVU×2	Down-counting GTDVU×2-1 to GTDVU	Up-counting GTDVU+1 to GTDVU×2
GPT32n+2.GTCNT	Stop 0	Up-counting 1 to GTDVU	Down-counting GTDVU-1 to 0

In complementary PWM mode, the GTCCRA register performs unusual buffer operation.

Data transfers from the GTCCRD register to the temporary register A and from the GTCCRF register to the temporary register B are performed at the same time in three channels by writing a value to the GTCCRD register of the GPT32n+2 channel.

Data transfers from the temporary register A and temporary register B to the GTCCRC and GTCCRE registers vary depending on the transfer timing to the temporary register A and temporary register B. Data transfers from the GTCCRC and GTCCRE registers to the GTCCRA register are performed according to each complementary PWM mode name (crest transfer, trough transfer, and crest/trough transfer).

Buffer operation of the GTPR register in complementary PWM mode is described in section 23.3.2.1. GTPR Register Buffer Operation. Do not perform buffer operation for the GTDVU register in complementary PWM mode.

Table 23.32 shows buffer transfer timing during single buffer operation in complementary PWM modes 1 to 3. Table 23.33 shows buffer transfer timing during double buffer operation in complementary PWM mode 3.

Table 23.32 Single Buffer Transfer Timing in Complementary PWM Mode 1, 2, 3

Buffer Transfer	Complementary PWM Mode 1	Complementary PWM Mode 2	Complementary PWM Mode 3 (Single Buffer)
GTCCRD ↓ Temporary register A	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register A ↓ GTCCRC	(1) When data is transferred to temporary register A in up-counting middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than up-counting middle section At the end of trough section	(1) When data is transferred to temporary register A in down-counting middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than down-counting middle section At the end of crest section	(1) When data is transferred to temporary register A in middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than middle section At the end of crest and trough sections
GTCCRC ↓ GTCCRA	At the end of crest section Counter clear in up-counting middle section and crest section	At the end of trough section (excluding initial output section) Counter clear in down-counting middle section and trough section	At the end of crest section At the end of trough section (excluding initial output section) Counter clear

Table 23.33 Double Buffer Transfer Timing in Complementary PWM Mode 3

Transfer from GTCCRD to GTCCRA		Transfer from GTCCRF to GTCCRA	
Buffer Transfer	**Transfer Timing**	**Buffer Transfer**	**Transfer Timing**
GTCCRD ↓ Temporary register A	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	GTCCRF ↓ Temporary register B	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register A ↓ GTCCRC	(1) When data is transferred to temporary register A in middle section After one GTCLK cycle from transfer to temporary register A (2) When data is transferred to temporary register A in a section other than middle section At the end of crest and trough sections	Temporary register B ↓ GTCCRE	(1) When data is transferred to temporary register B in middle section After one GTCLK cycle from transfer to temporary register B (2) When data is transferred to temporary register B in a section other than middle section At the end of crest and trough sections
GTCCRC ↓ GTCCRA	At the end of crest section Counter clear	GTCCRE ↓ GTCCRA	At the end of trough section (excluding initial output section)

An output level change in the positive-phase waveform from the GTIOCn+iA pin (i = 0, 1, 2) and the negative-phase waveform from the GTIOCn+iB pin occurs at a compare match in combination of counters and registers determined for each operation section. In middle sections, the positive-phase waveform output level changes at a compare match of the GPT32n.GTCNT counter and the GTCCRA register, and the negative-phase waveform output level changes at a compare match between the GPT32n+1.GTCNT counter and the GTCCRA register. In crest and trough sections, compare match operation is performed using the GPT32n+2.GTCNT counter, GTCCRC register, and GTCCRE register to ensure the linearity in the vicinity of duty 0% and 100%.

In the case that the compare match value equals to or larger than the GPT32n.GTPR register value, the duty becomes 0% (positive-phase waveform OFF, negative-phase waveform ON). In the case that the compare match value is 0, the duty becomes 100% (positive-phase waveform ON, negative-phase waveform OFF).

Table 23.34 lists combinations of counters and registers used for compare match operation to generate a positive-phase waveform and a negative-phase waveform in each operation section.

Table 23.34 Combinations of Counters and Registers for Compare Match Operation in Complementary PWM Mode

	Up-Counting Middle Section	Up-Counting Crest Section	Down-Counting Crest Section	Down-Counting Middle Section	Down-Counting Trough Section	Up-Counting Trough Section
Negative-phase OFF	GPT32n+1.GTCNT	GPT32n+1.GTCNT	—	GPT32n+2.GTCNT*1	GPT32n+2.GTCNT	GPT32n+1.GTCNT
	GTCCRA	GTCCRA	—	GTCCRC (GTCCRE for double buffer operation)	GTCCRC (GTCCRE for double buffer operation)	GTCCRC (GTCCRE for double buffer operation)
Positive-phase ON	GPT32n.GTCNT	GPT32n.GTCNT	GPT32n+2.GTCNT	—	GPT32n.GTCNT *1	GPT32n.GTCNT
	GTCCRA	GTCCRA	GTCCRA	—	GTCCRC (GTCCRE for double buffer operation)	GTCCRC (GTCCRE for double buffer operation)
Positive-phase OFF	GPT32n+2.GTCNT*1	GPT32n+2.GTCNT	GPT32n.GTCNT	GPT32n.GTCNT	GPT32n.GTCNT	—
	GTCCRC	GTCCRC	GTCCRC	GTCCRA	GTCCRA	—
Negative-phase ON	—	GPT32n+1.GTCNT*1	GPT32n+1.GTCNT	GPT32n+1.GTCNT	GPT32n+1.GTCNT	GPT32n+2.GTCNT
	—	GTCCRC	GTCCRC	GTCCRA	GTCCRA	GTCCRA

Note 1. Compare match is performed only at the time of final count in the target section, but is not performed at count values other than the final count.

In the case of normal complementary PWM mode waveform, a PWM waveform change occurs in the order of negative-phase OFF → positive-phase ON → positive-phase OFF → negative-phase ON. However, this order may vary depending on operation section and register values. In this case, OFF takes precedence in trough sections and ON takes precedence in crest sections (for negative-phase waveforms), and ON takes precedence in trough sections and OFF takes precedence in crest sections (for positive-phase waveforms). A lower-priority compare match that occurs at the same time or after a higher-priority compare match is ignored.

In the initial output section, the initial output set in the GTIOR register is retained. In the case that the GTCCRA register value is larger than the GTDVU register value at the end of the initial output section, negative phase is enabled. In the case that the GTCCRA register value is not larger than the GTDVU register value, positive phase is enabled.

As operation examples of normal complementary PWM mode waveform where compare match operation occurs in the middle section, Figure 23.45 and Figure 23.46 show complementary PWM mode 1, Figure 23.47 and Figure 23.48 show complementary PWM mode 2, Figure 23.49 and Figure 23.50 show single buffer complementary PWM mode 3, and Figure 23.51 and Figure 23.52 show double buffer complementary PWM mode 3.

Figure 23.53 to Figure 23.64 show complementary PWM mode waveforms where compare match operation occurs in crest sections and trough sections and differences due to compare match occurrence order.

Figure 23.65 and Figure 23.66 show examples of initial output operation according to the GTCCRA register value.

Table 23.35 shows an example for setting complementary PWM modes 1 to 3.

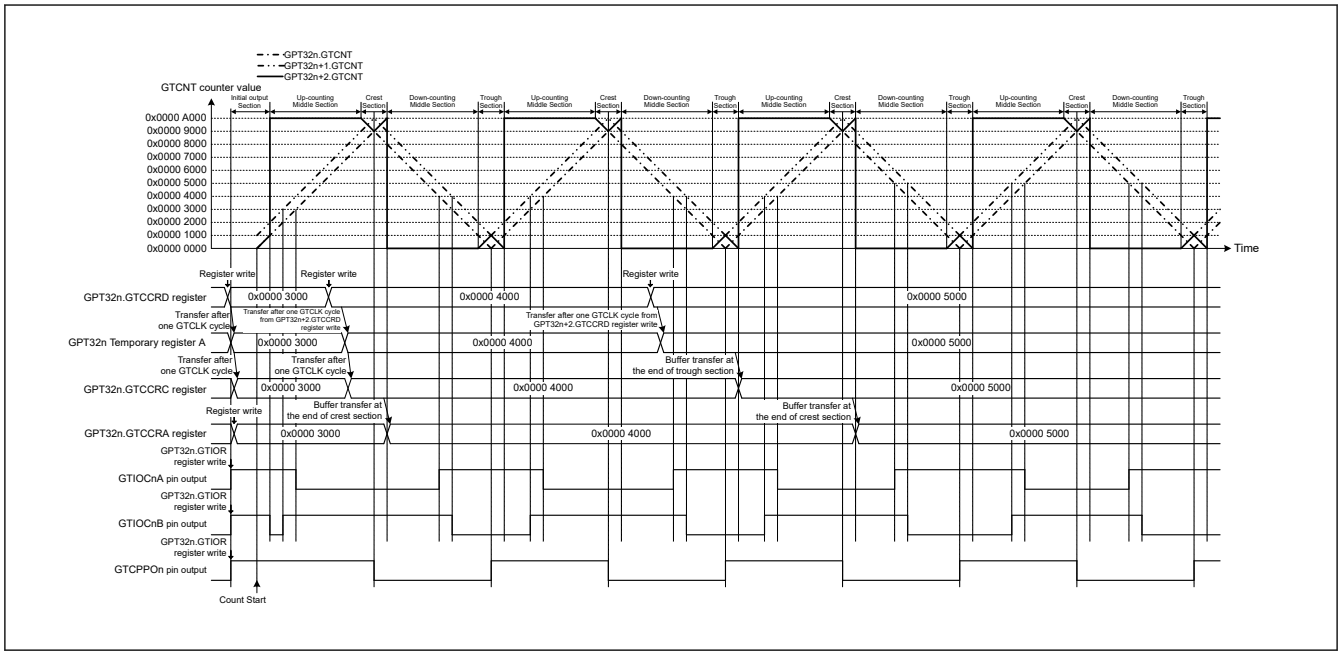


Figure 23.45 Example of Complementary PWM Mode 1 Operation (GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)

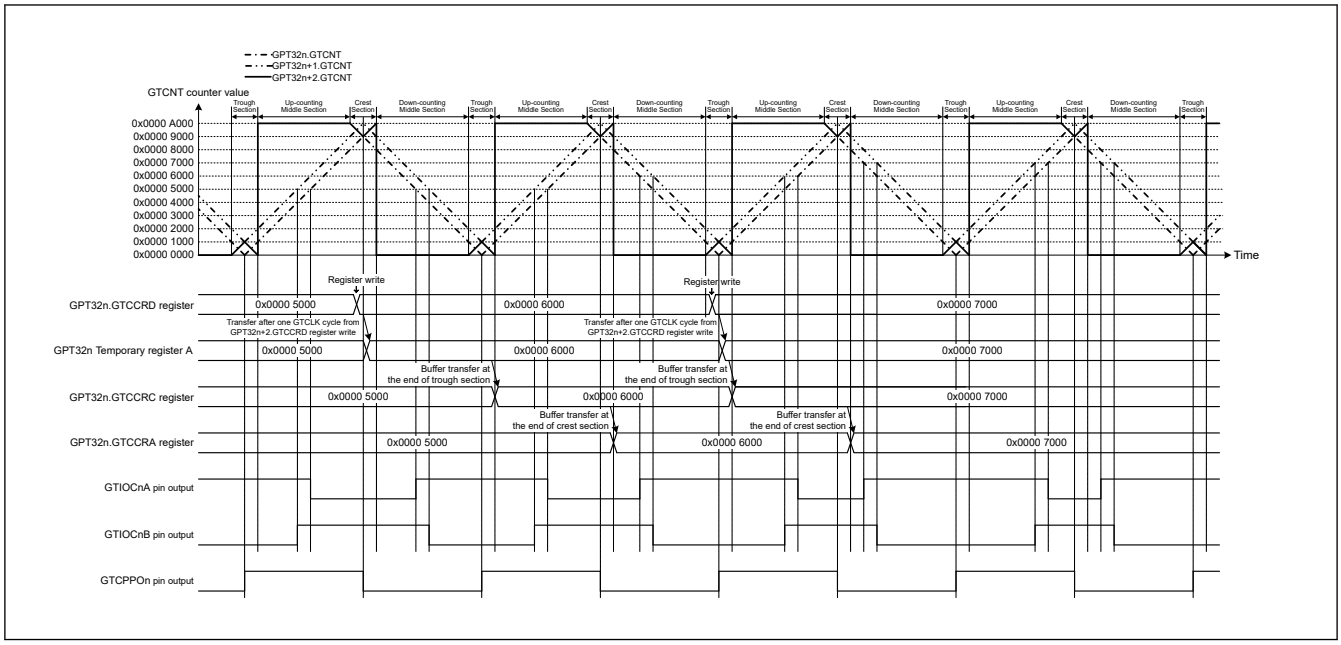


Figure 23.46 **Example of Complementary PWM Mode 1 Operation (GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)**

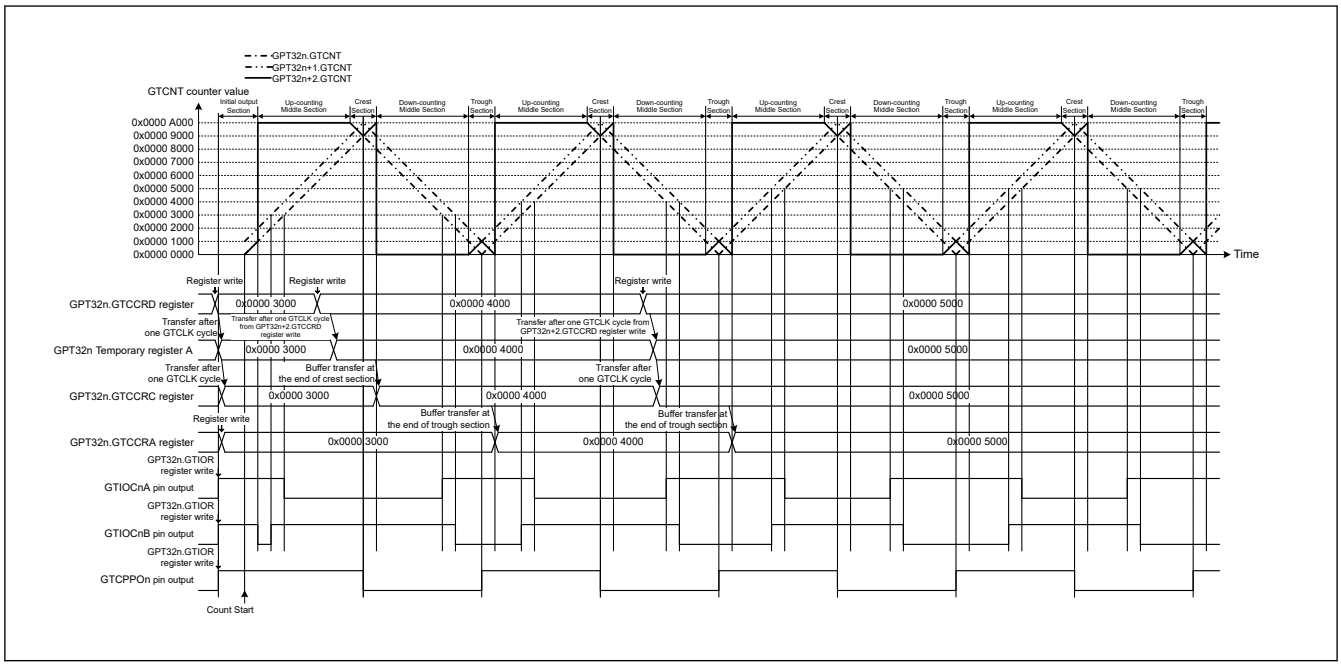


Figure 23.47 **Example of Complementary PWM Mode 2 Operation (GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)**

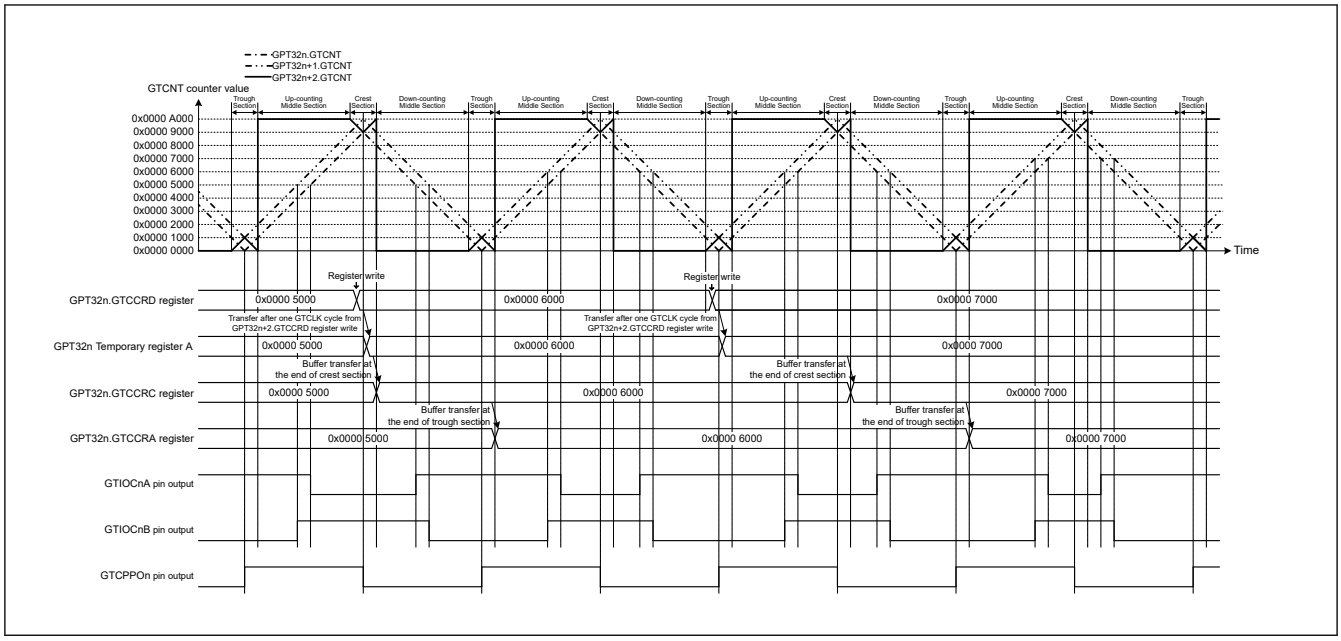


Figure 23.48 **Example of Complementary PWM Mode 2 Operation (GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)**

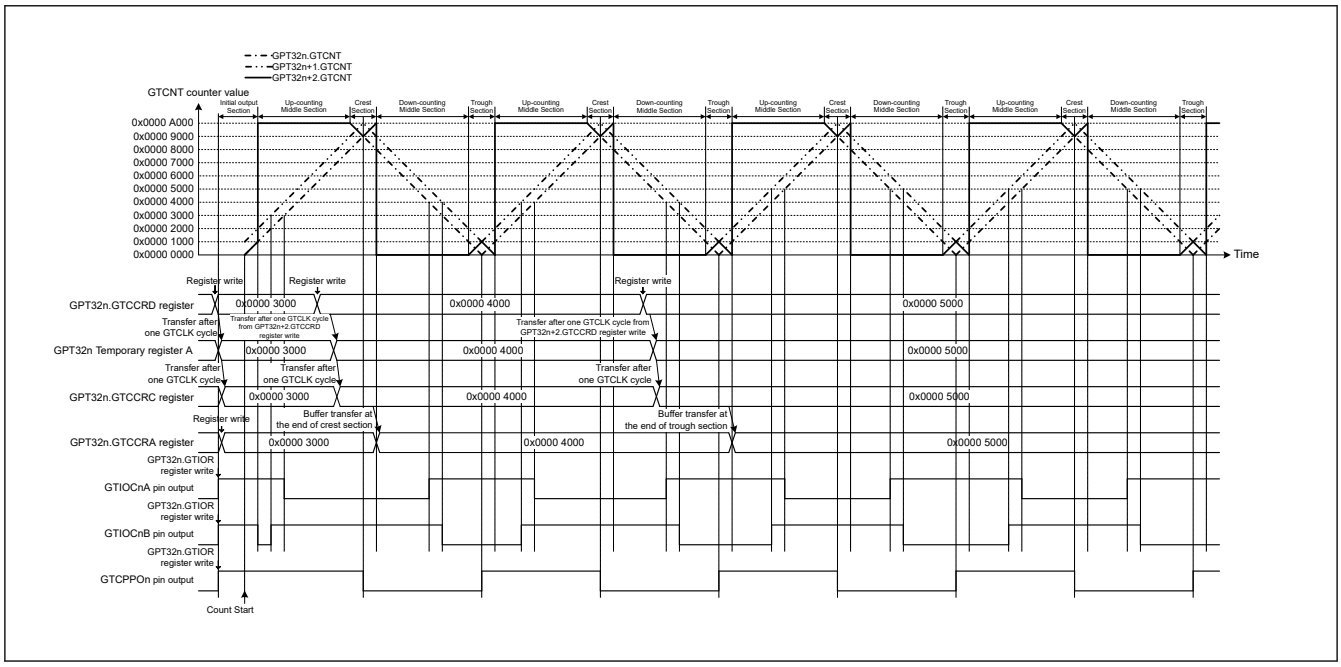


Figure 23.49 **Example of Complementary PWM Mode 3 Operation (Single buffer operation, GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)**

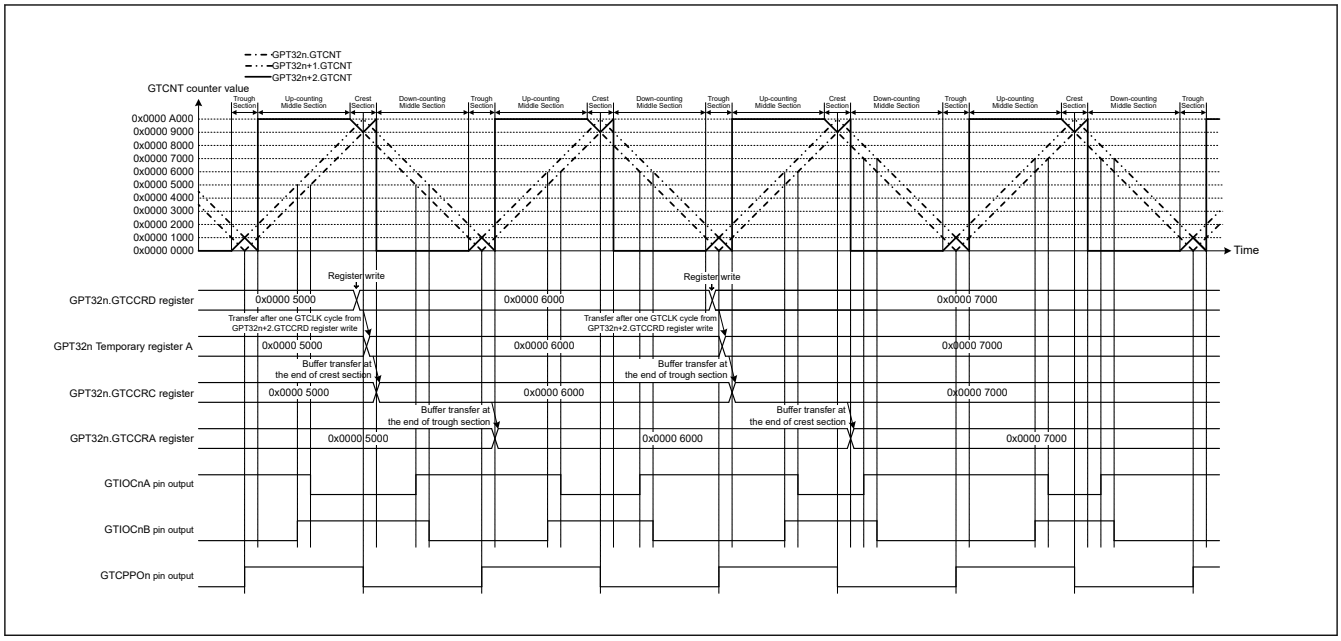


Figure 23.50 **Example of Complementary PWM Mode 3 Operation (Single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)**

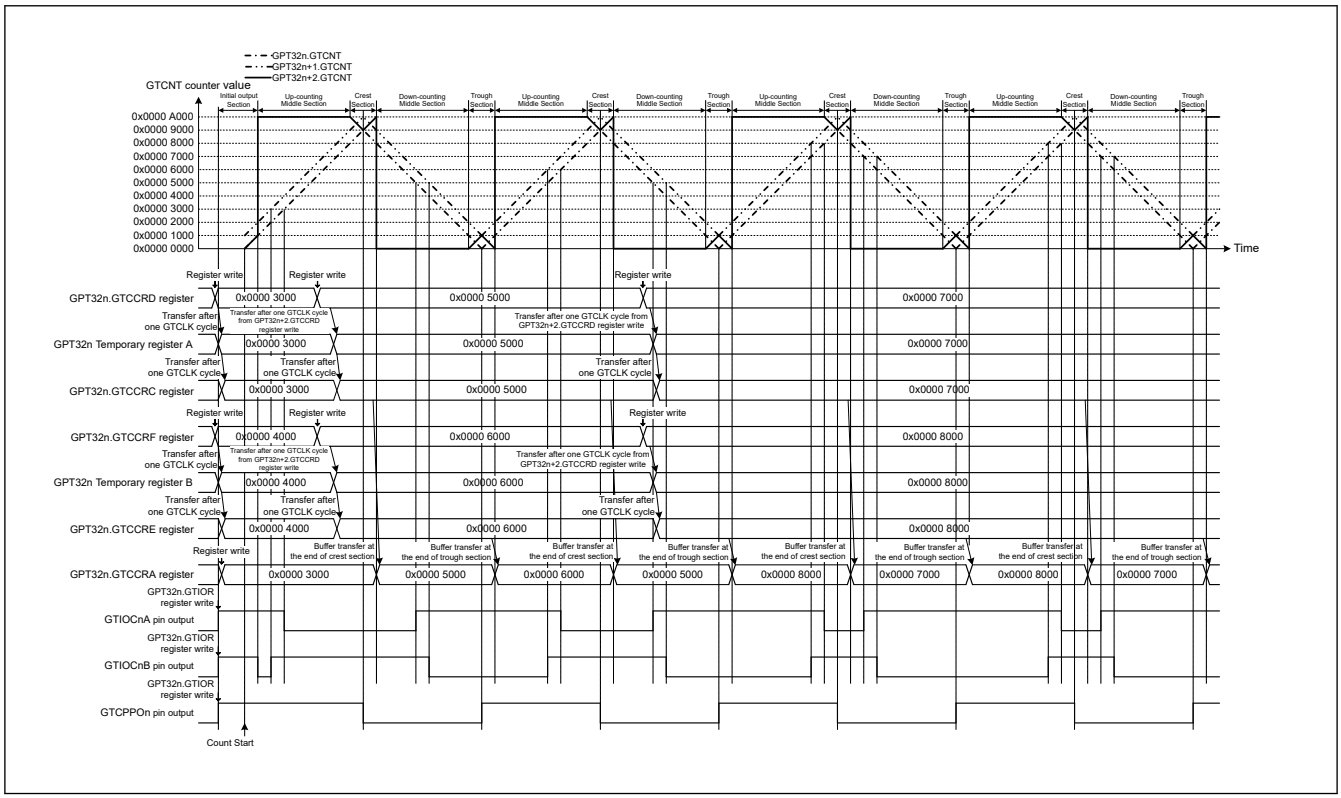


Figure 23.51 **Example of Complementary PWM Mode 3 Operation (Double buffer operation, GTIOCnA pin = High / GTIOCnB pin = High as initial output, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in middle section) (n = 4, 7)**

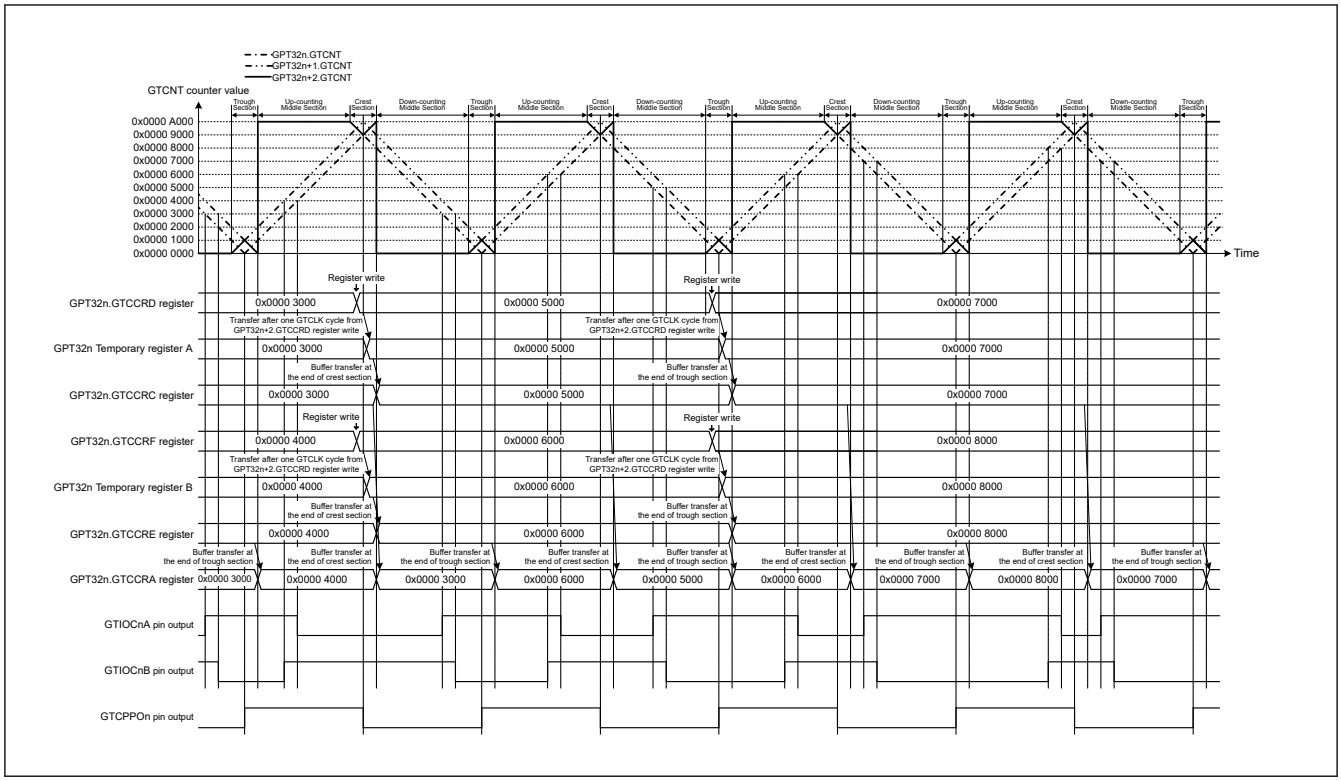


Figure 23.52 Example of Complementary PWM Mode 3 Operation (Double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000 and updating GTCCRD register in crest and trough sections) (n = 4, 7)

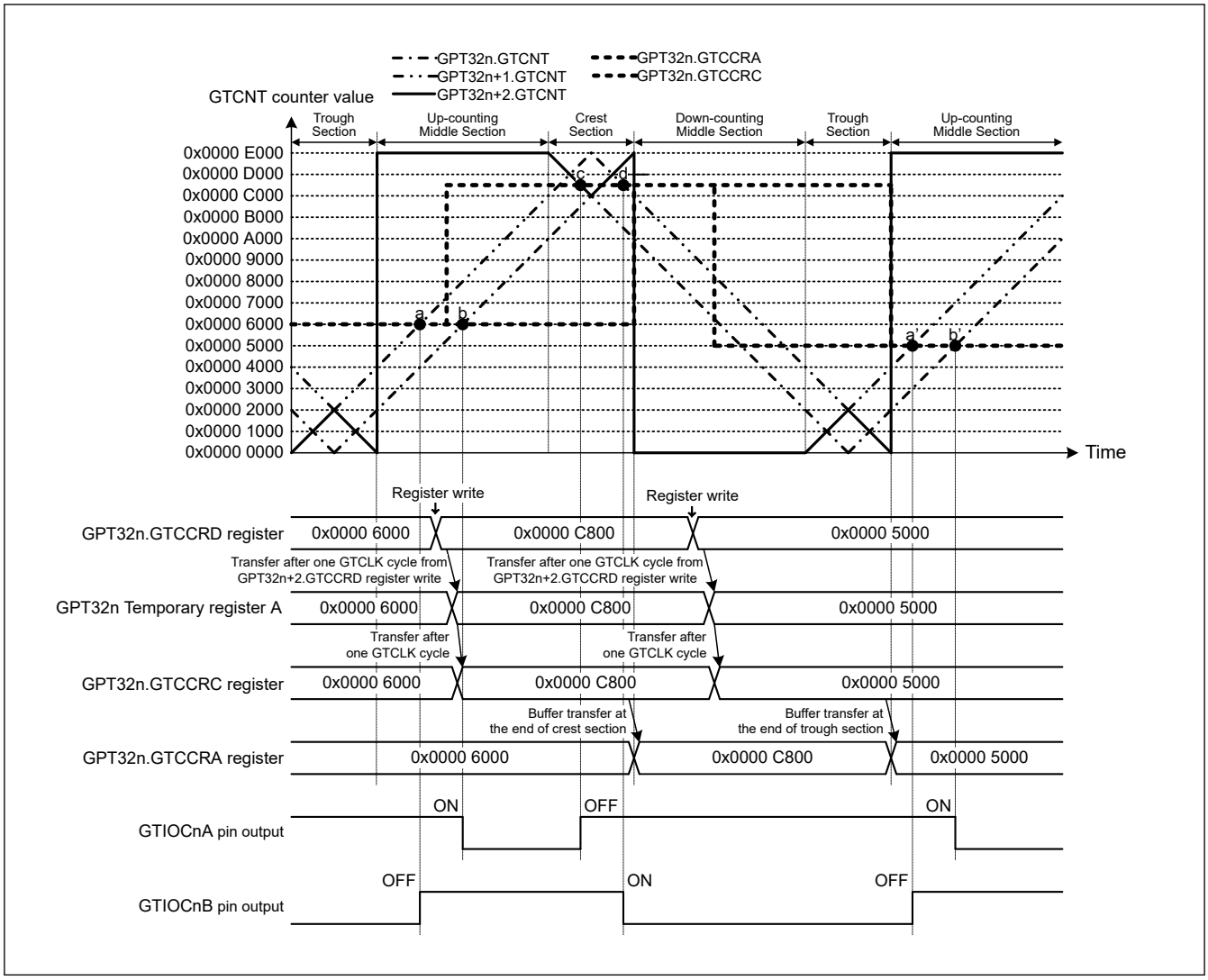


Figure 23.53 **Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a → b → c → d) (n = 4, 7)**

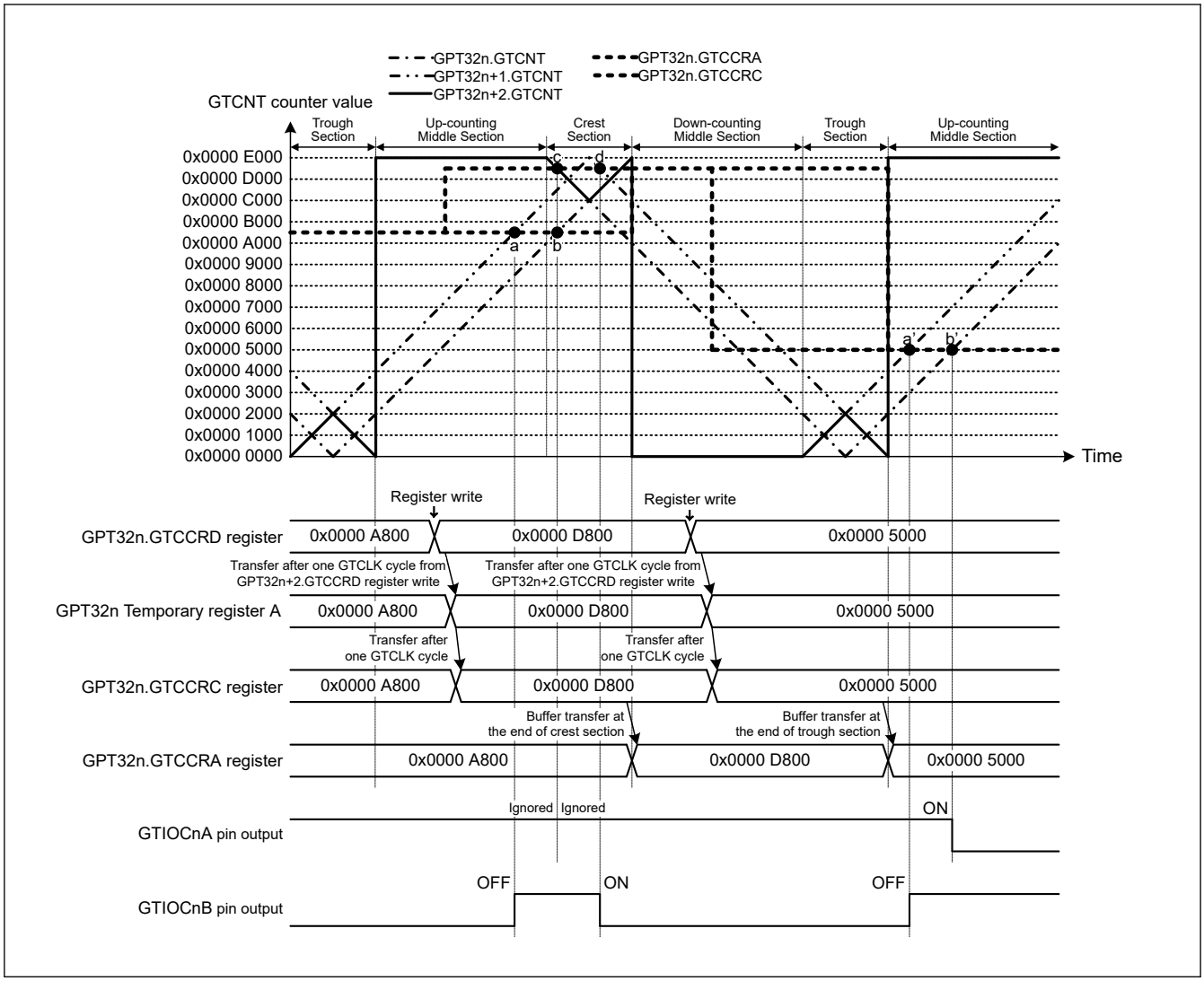


Figure 23.54 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a → (b, c) → d) (n = 4, 7)

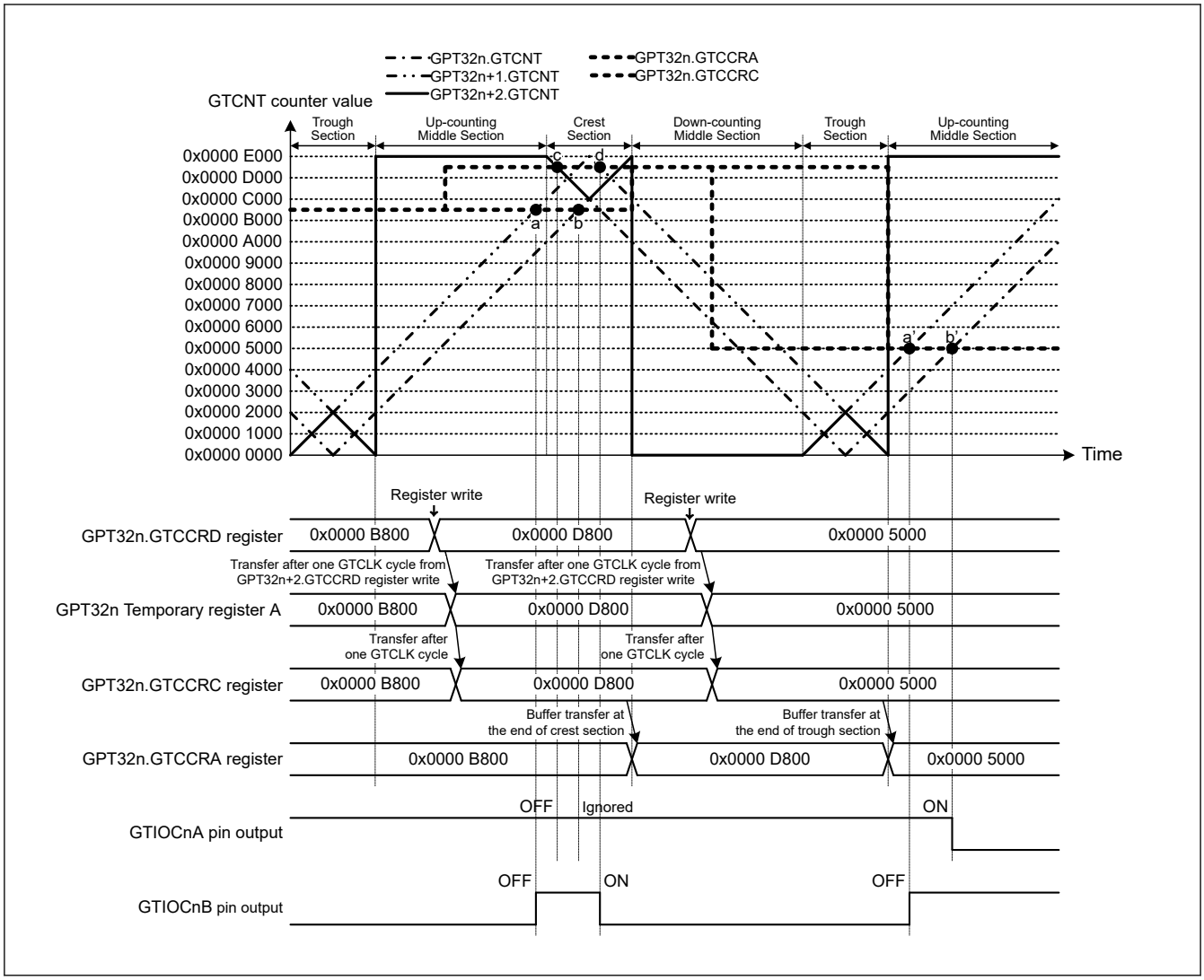


Figure 23.55 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a → c → b → d) (n = 4, 7)

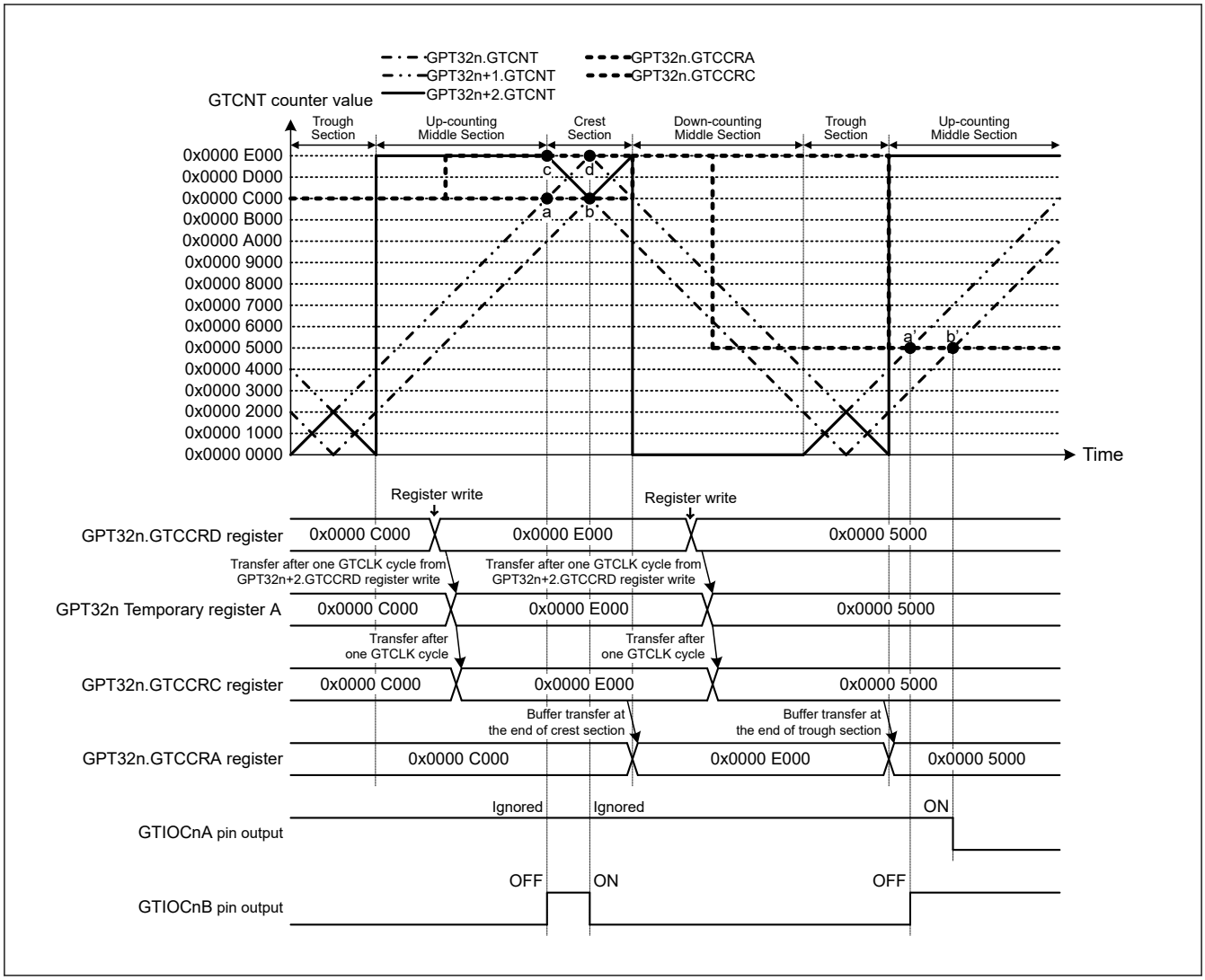


Figure 23.56 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: (a, c) → (b, d)) (n = 4, 7)

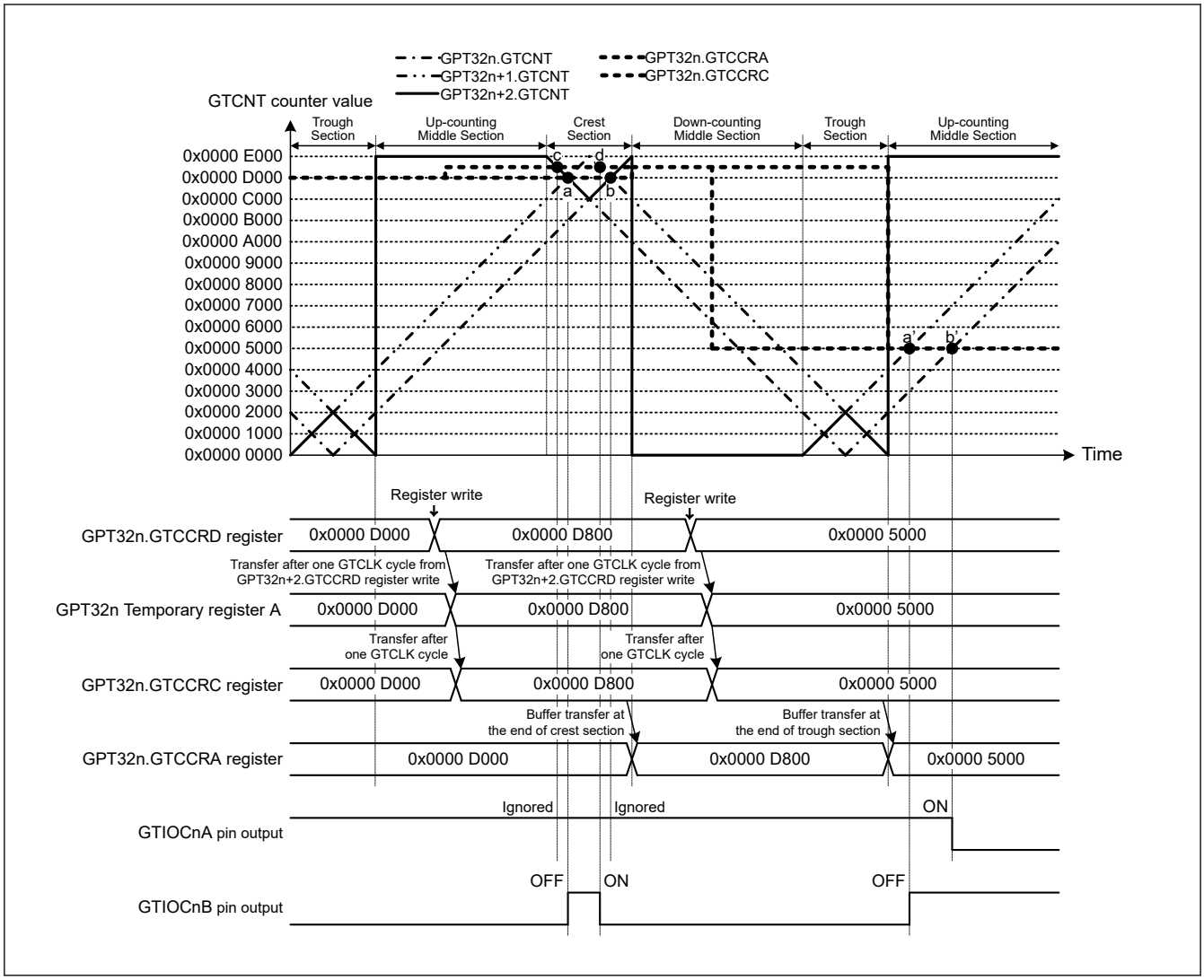


Figure 23.57 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → a → d → b) (n = 4, 7)

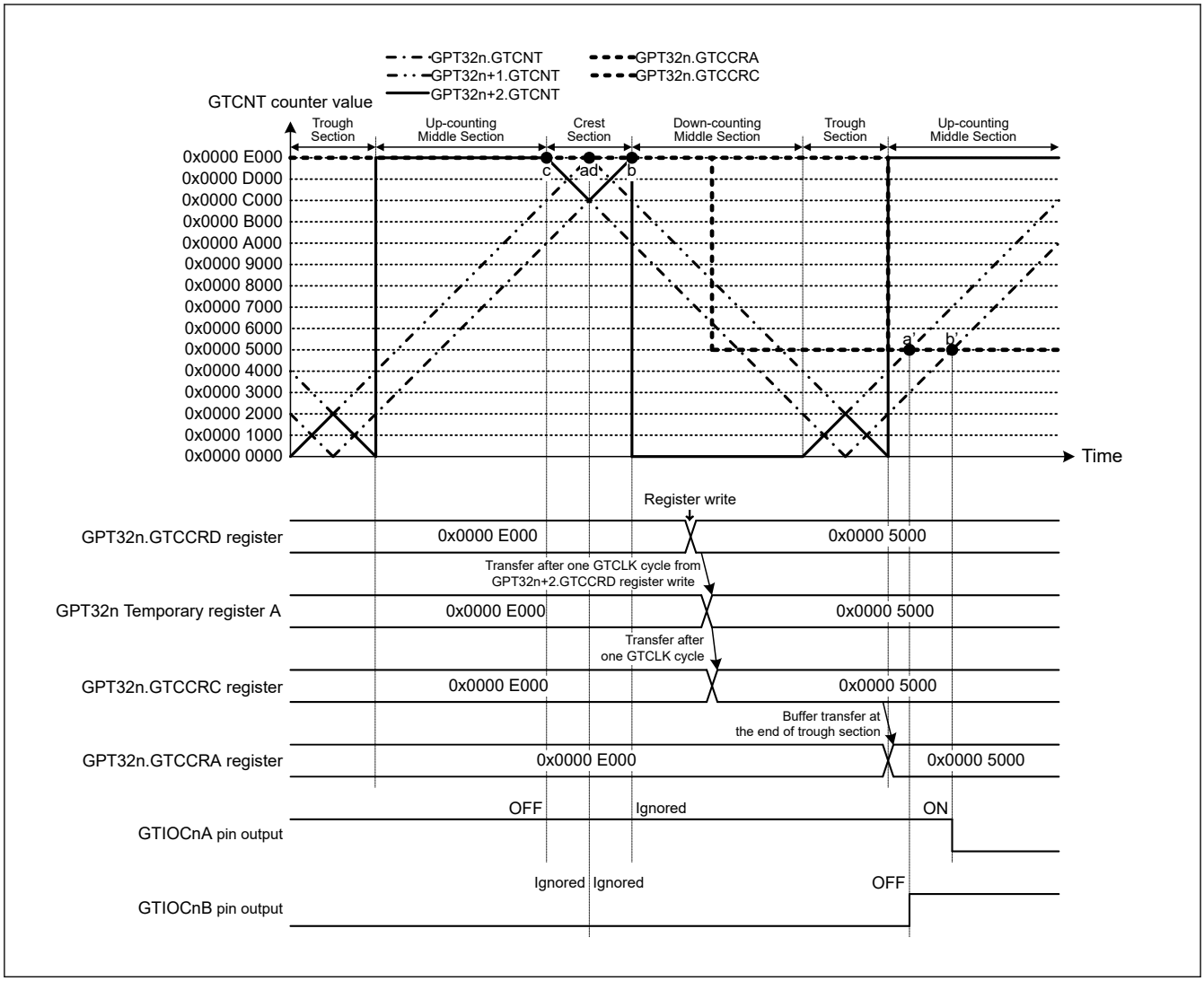


Figure 23.58 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → (a, d) → b) (n = 4, 7)

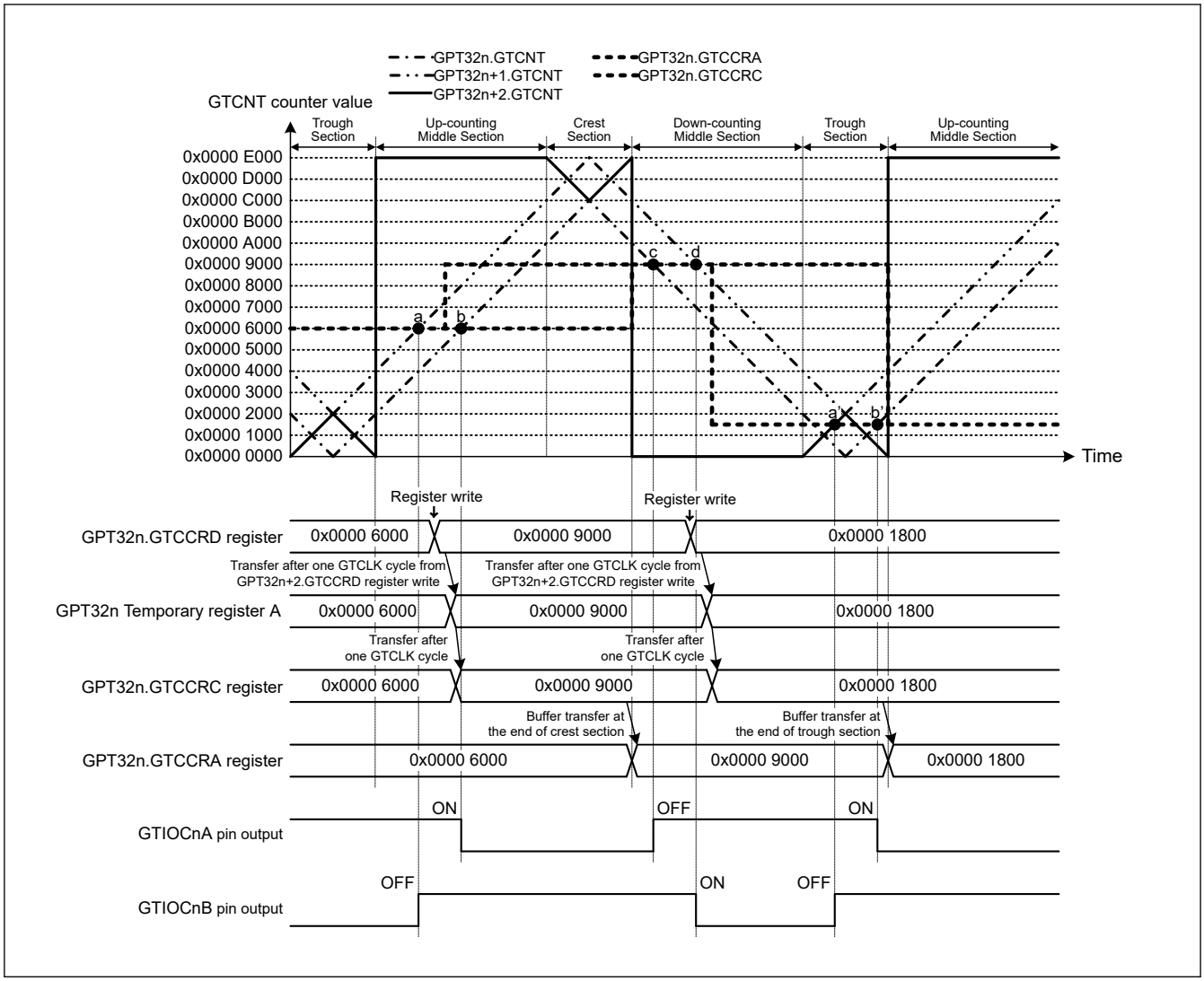


Figure 23.59 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → d → a' → b') (n = 4, 7)

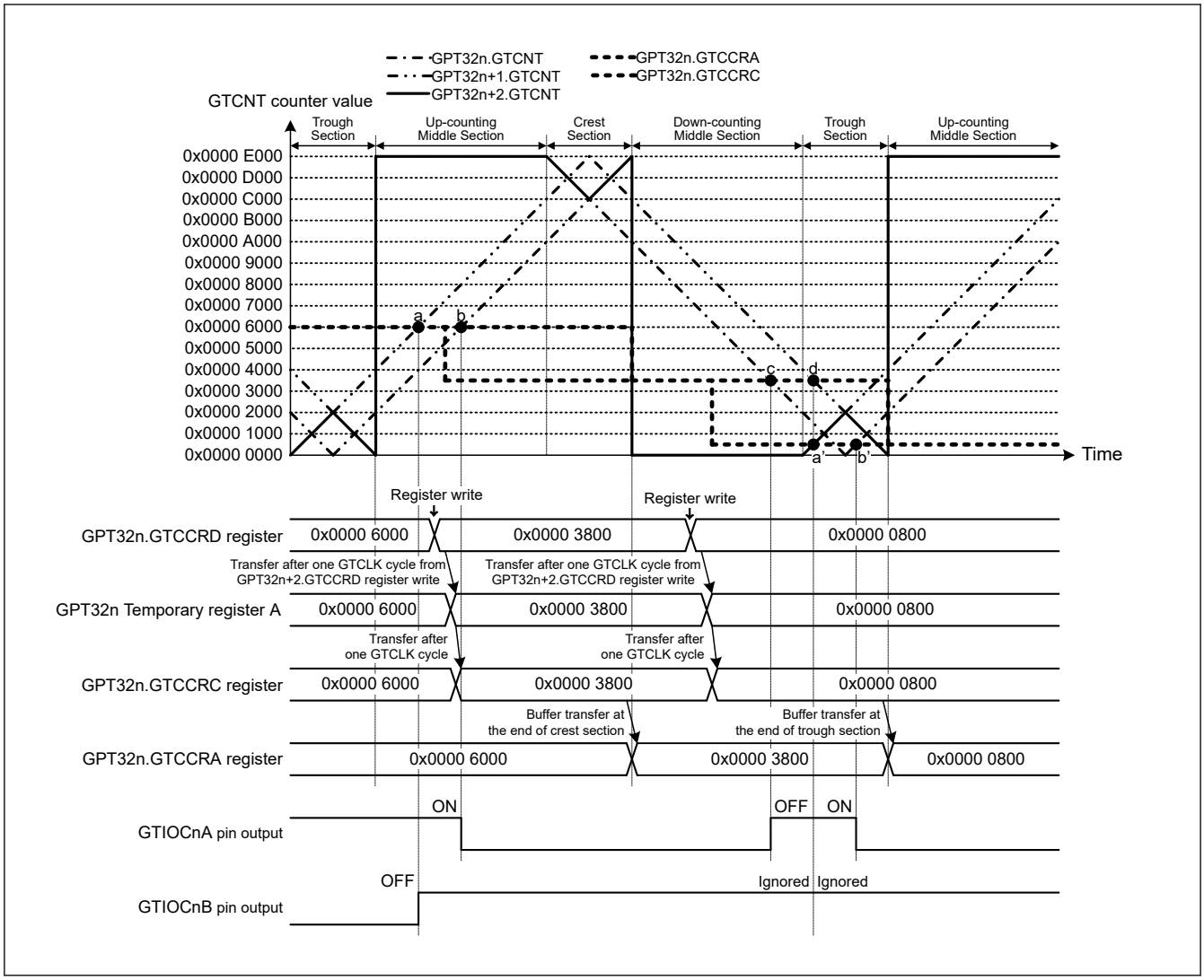


Figure 23.60 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → (d, a') → b') (n = 4, 7)

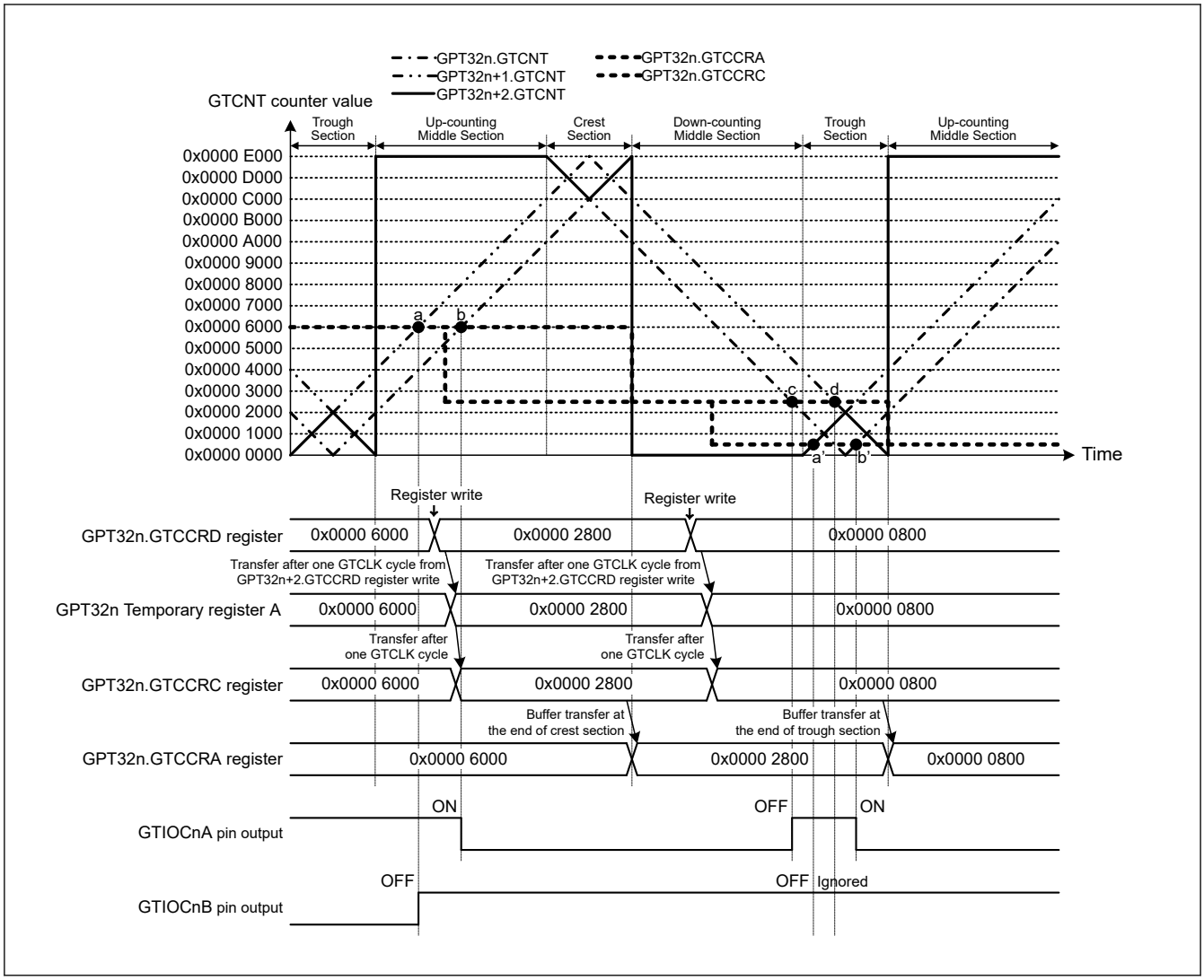


Figure 23.61 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: c → a' → d → b') (n = 4, 7)

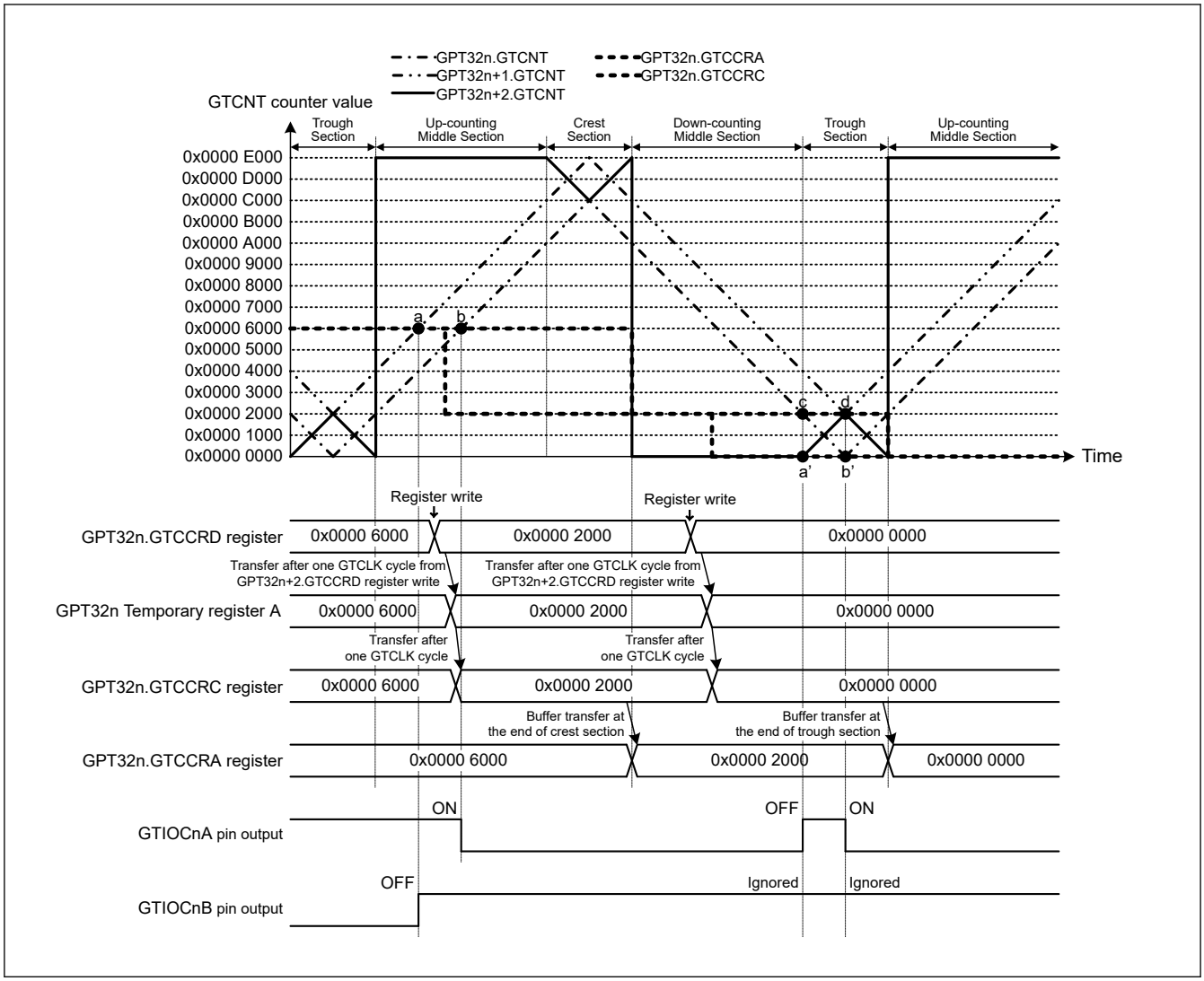


Figure 23.62 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: (c, a') → (d, b')) (n = 4, 7)

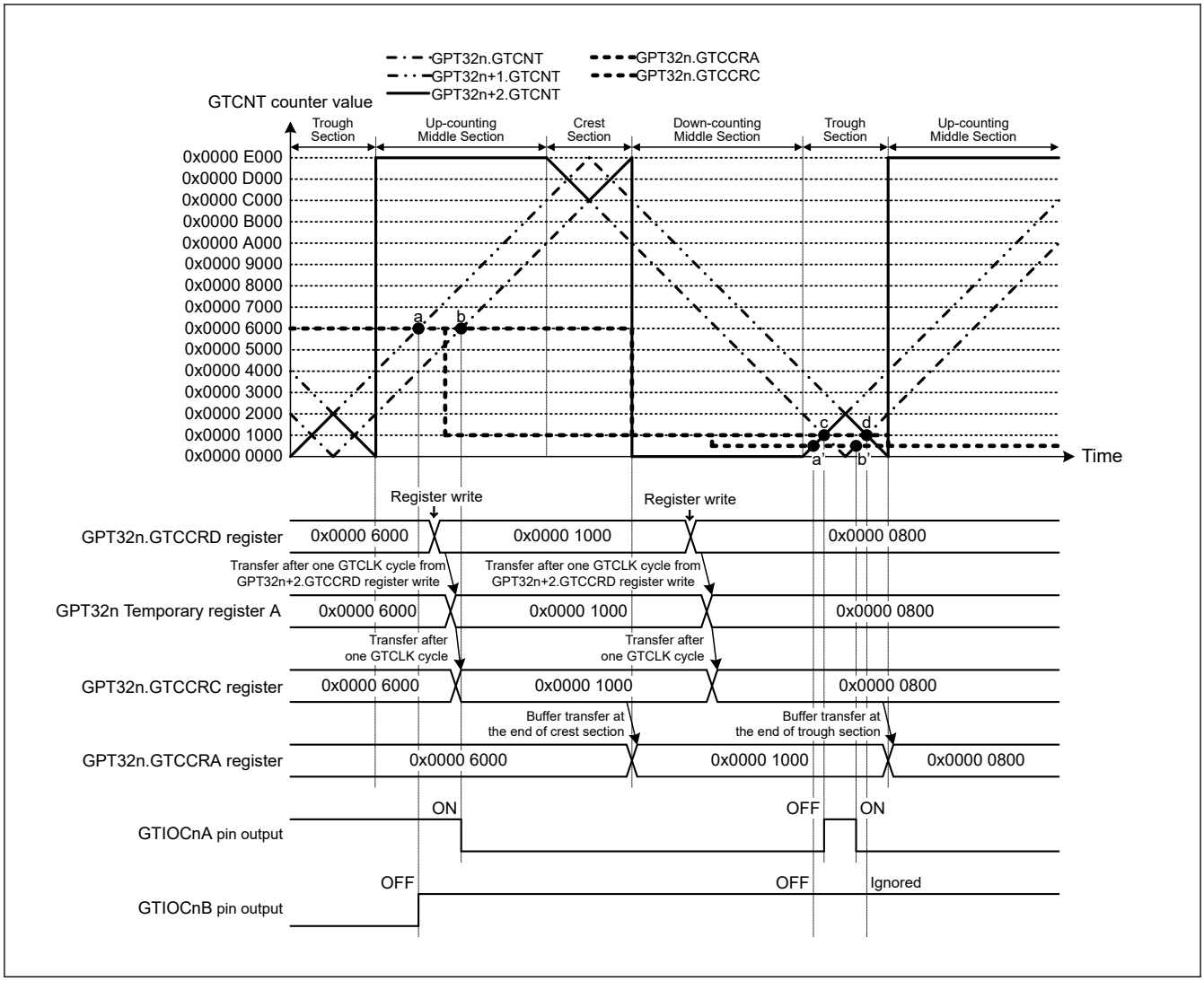


Figure 23.63 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a' → c → b' → d) (n = 4, 7)

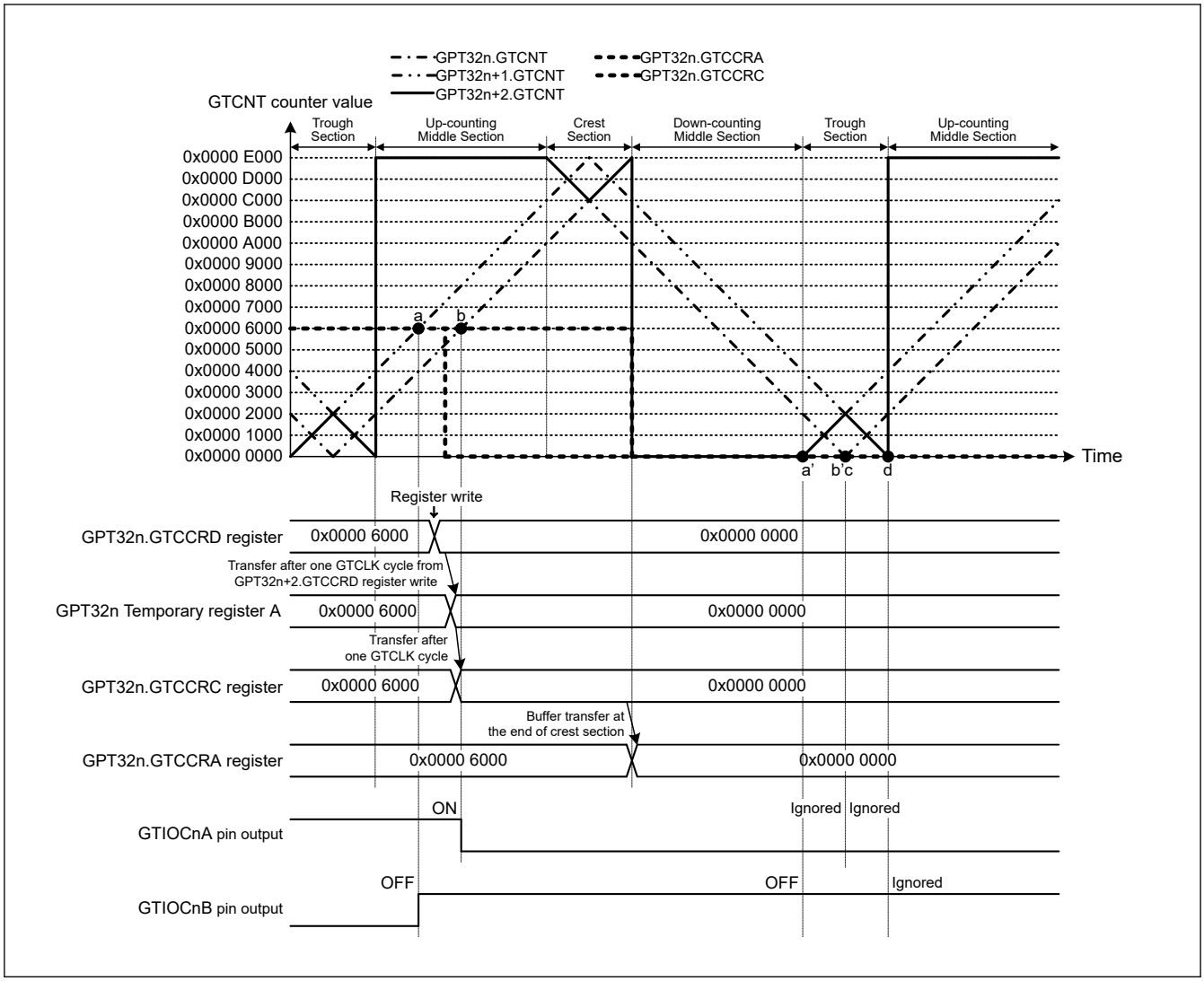


Figure 23.64 Example of Compare Match Generation Sequence Operation in Complementary PWM Mode (Complementary PWM mode 3 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 2000, compare match generation order: a' → (b', c) → d) (n = 4, 7)

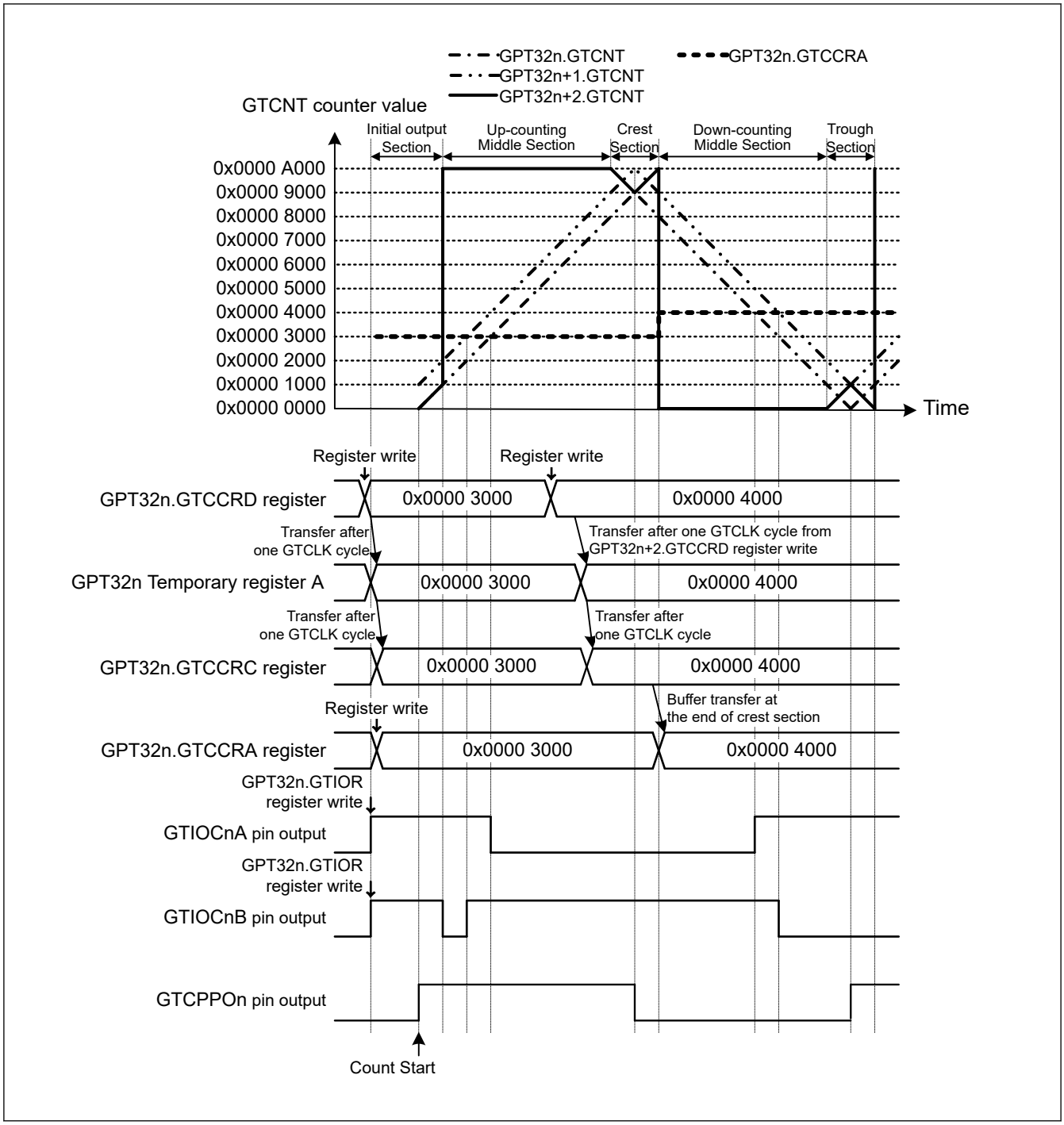


Figure 23.65 **Example of Complementary PWM Mode Initial Output Operation (Complementary PWM mode 1 operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000, in the case that the initial GTCCRA register value is larger than the dead time value) (n = 4, 7)**

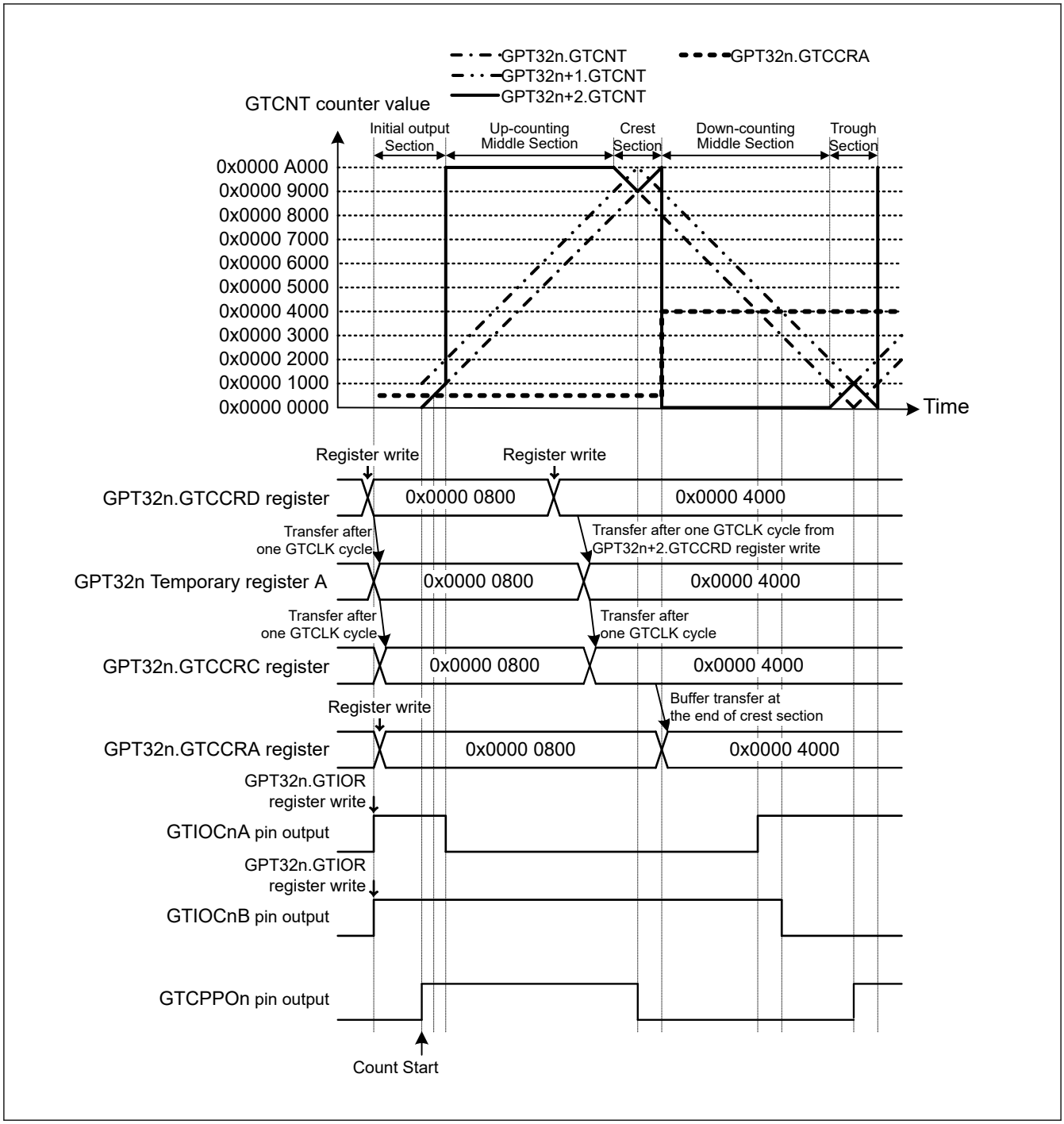


Figure 23.66 **Example of Complementary PWM Mode Initial Output Operation (Complementary PWM mode 1 operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, the dead time value is 0x0000 1000, in the case that the initial GTCCRA register value is equal to or less than the dead time value) (n = 4, 7)**

Table 23.35 **Example for Setting Complementary PWM Mode 1, 2, 3 (1 of 2)**

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0] bits of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in the GPTWn.GTPR, GPTWn.GTPBR and GPTWn.GTPDBR register.

Table 23.35 Example for Setting Complementary PWM Mode 1, 2, 3 (2 of 2)

No.	Step Name	Description
4	Set GTIOCnm /GTIOCn+1m / GTIOCn+2m pin function	Set the function of the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
5	Enable GTCPPOn pin output	Set to enable or disable PWM synchronous output from the GTCPPOn pin with the PSYE bit in the GTIOR register of the GPT32n channel.
6	Enable GTIOCnm / GTIOCn+1m /GTIOCn+2m pin output	Set to enable the output from the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with the OAE and OBE bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
7	Set buffer operation	In complementary PWM mode 3, set buffer operation with the GTBER2.CP3DB bit of the GPT32n, GPT32n+1, and GPT32n+2 channels.
8	Set compare match value	Set the output pin changing point during up-counting after count start in the GTCCRA register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
9	Set buffer value	For single buffer operation, set data (to be transferred for the first buffer transfer to the GTCCRA register after count start) in the GTCCRD register. For buffer operation in complementary PWM mode 2, set the same value as the GTCCRA register in the GTCCRD register because the first buffer transfer does not take place. For double buffer operation in complementary PWM mode 3, set data to be transferred at the first end of crest in the GTCCRD register and set data to be transferred at the first end of trough in the GTCCRF register.
10	Set dead time value	Set the dead time value in GTDVU of GTP32n channel.
11	Start count operation	Set GTCR.CST of GPT32n channel to 1 to start count operation.
12	Set buffer value for each cycle	For single buffer operation, set data (to be transferred for the next buffer transfer to the GTCCRA register) in the GTCCRD register. For double buffer operation in complementary PWM mode 3, set data to be transferred for the next buffer transfer in the GTCCRF register. Make settings for the GPT32n+2.GTCCRD register finally. (Data is transferred to the temporary register.)

Note: n = 4, 7
m = A, B

23.3.3.8 Complementary PWM mode 4

In complementary PWM mode 4, the value written to the GTCCRD and GTCCRF registers is immediately applied to compare match operation by transferring data also to the GTCCRA register during buffer transfer to a temporary register before crest or trough transfer timing.

Figure 23.67 shows the block diagram in complementary PWM mode 4.

In the configuration of complementary PWM mode 4, a buffer transfer path from the GTCCRD register to the GTCCRC and GTCCRA registers and a buffer transfer path from the GTCCRF register to the GTCCRE and GTCCRA registers are added to other complementary PWM modes shown in Table 23.35.

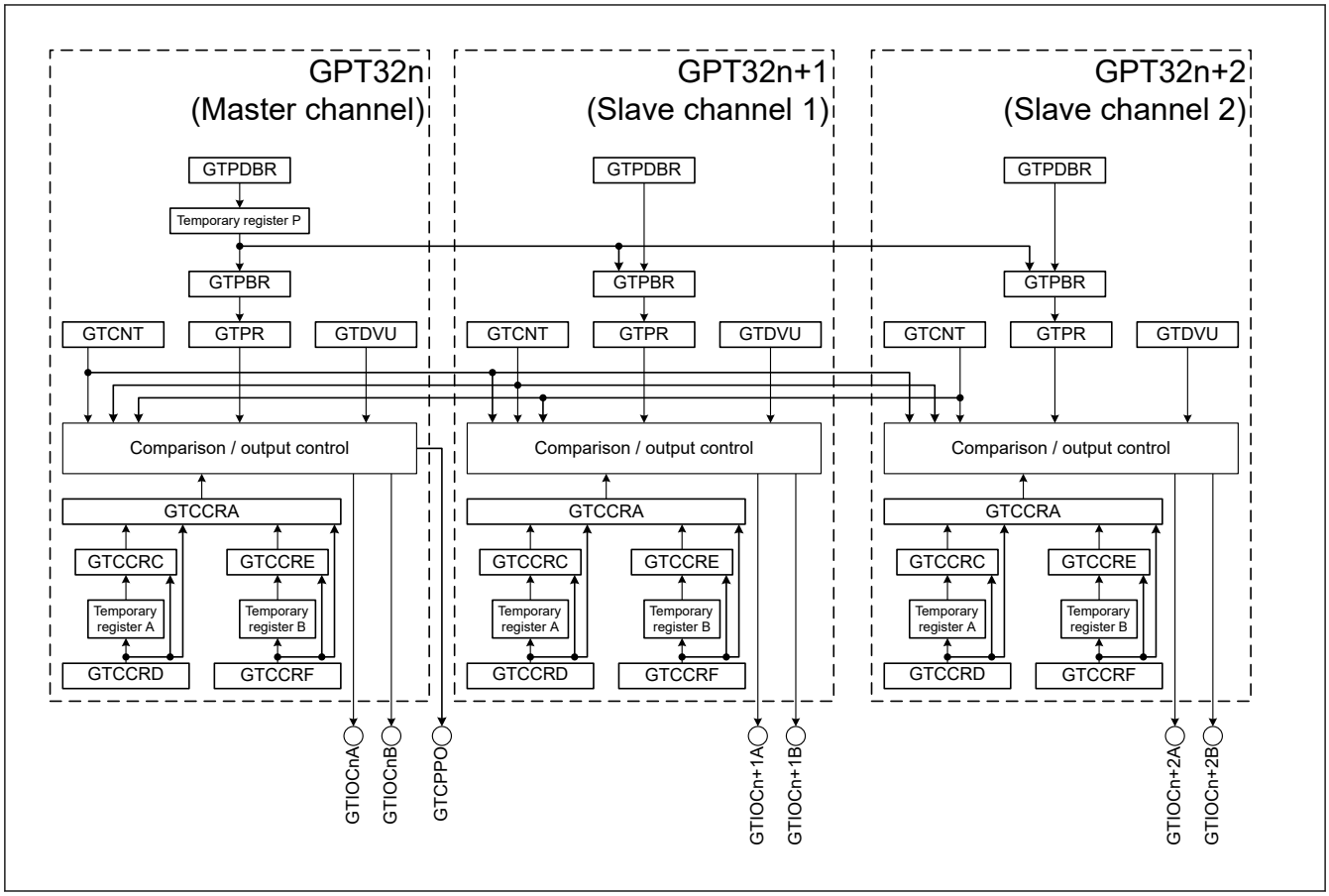


Figure 23.67 Block Diagram in Complementary PWM Mode 4 (n = 4, 7)

Count operation is performed in the same way as complementary PWM modes 1 to 3. See Table 23.30 and Table 23.31.

With respect to buffer operation and PWM waveform changes in complementary PWM mode 4, buffer transfer (shown in Figure 23.67) from the GTCCRD and GTCCRF registers is added based on the complementary PWM mode 3 operation. Buffer transfer and PWM waveform are controlled according to operation section, state of comparison with the GTCCRA register, and write value.

The double buffer function by writing to the GTCCRF register can be enabled or disabled with the GTBER2.CP3DB bit. In double buffer operation, the value written to the GTCCRD register is used as a compare match value for positive-phase OFF (negative-phase ON) during down-counting, and the value written to the GTCCRF register is used as a compare match value for negative-phase OFF (positive-phase ON) during up-counting. Transfer register, transfer value, and PWM output changes are controlled by operation section (where the value is written), state of comparison with the GTCCRA register, and write value.

Double buffer operation is guaranteed only in the up-counting middle section and down-counting middle section. Setting a value not larger than the dead time value and not less than the count cycle is prohibited.

In single buffer operation, a compare match value is written only to the GTCCRD register, and transfer register, transfer value, and PWM output changes are controlled by operation section (where the value is written), state of comparison with the GTCCRA register, and write value.

Transfer from the GTCCRD register to the temporary register A and transfer from the GTCCRF register to the temporary register B are performed in the same way as other complementary PWM modes. Transfers are concurrently performed in three channels by writing a value to the GPT32n+2.GTCCRD register. Transfer from the GTCCRD register to the GTCCRC register, GTCCRA register, temporary register B, and GTCCRE register and transfer from the GTCCRF register to the GTCCRE register and the GTCCRA register are performed at the same time as the above-mentioned transfer to the temporary register.

Table 23.36 and Table 23.37 show immediate buffer transfer (for transfer to the temporary register by writing a value to the GPT32n+2.GTCCRD register) to the GTCCRC and GTCCRA registers by writing a value to the GTCCRD register during single buffer operation in complementary PWM mode 4 for each compare match state in each operation section. Transfers (from the GTCCRD register to the temporary register A, from the temporary register A to the GTCCRC register, and from

the GTCCRC register to the GTCCRA register) other than those shown in Table 23.36 and Table 23.37 are the same as single buffer transfer in complementary PWM mode 3 shown in Table 23.32.

Table 23.38 and Table 23.39 show immediate buffer transfer (for transfer to the temporary register by writing a value to the GPT32n+2.GTCCRD register) to each register by writing a value to the GTCCRD and GTCCRF registers during double buffer operation in complementary PWM mode 4 for each compare match state in each operation section. Transfers (from the GTCCRD register to the temporary register A, from the GTCCRF register to the temporary register B, from the temporary register A to the GTCCRC register, from the temporary register B to the GTCCRE register, and from the GTCCRC and GTCCRE registers to the GTCCRA register) other than those shown in Table 23.38 and Table 23.39 are the same as double buffer transfer in complementary PWM mode 3 shown in Table 23.33.

Table 23.36 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (1 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Up- counting middle section	Before up-counting compare match	GTCCRD	(i) In the case of GTCCRD > GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF
	Up-counting dead time period	GTCCRD	No transfer
	After up-counting compare match	GTCCRD	No transfer
Up-counting crest section	Before up-counting compare match	Before down-counting compare match GTCCRD After down-counting dead time start No transfer	Before down-counting compare match (i) In the case of GTCCRD > GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF After down-counting dead time start No transfer
	Up-counting dead time period	Before down-counting compare match GTCCRD After down-counting dead time start No transfer	No transfer
	After up-counting compare match	Before down-counting compare match (i) In the case of GTCCRD < GPT32n+2.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n+2.GTCNT GPT32n+2.GTCNT Positive-phase OFF After down-counting dead time start No transfer	No transfer

Table 23.36 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (2 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Down-counting crest section	Before down-counting compare match	Up-counting dead time period (i) In the case of GTCCRD < GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n+1.GTCNT GPT32n+1.GTCNT Negative-phase ON After up-counting compare match (i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF	No transfer
	Down-counting dead time period	No transfer	No transfer
	After down-counting compare match	No transfer	No transfer

Table 23.37 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (1 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Down-counting middle section	Before down-counting compare match	GTCCRD	(i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF
	Down-counting dead time period	GTCCRD	No transfer
	After down-counting compare match	GTCCRD	No transfer

Table 23.37 Immediate Single Buffer Transfer from GTCCRD Register in Complementary PWM Mode 4 (2 of 2)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
Down-counting trough section	Before down-counting compare match	Before up-counting compare match GTCCRD After up-counting dead time start No transfer	Before up-counting compare match (i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD = > GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF After up-counting dead time start No transfer
	Down-counting dead time period	Before up-counting compare match GTCCRD After up-counting dead time start No transfer	No transfer
	After down-counting compare match	Before up-counting compare match (i) In the case of GTCCRD > GPT32n+2.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n+2.GTCNT GPT32n+2.GTCNT Negative-phase OFF After up-counting dead time start No transfer	No transfer
Up- counting trough section	Before up-counting compare match	Down-counting dead time period (i) In the case of GTCCRD > GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n.GTCNT GPT32n.GTCNT Positive-phase ON After down-counting compare match (i) In the case of GTCCRD > GPT32n+1.GTCNT GTCCRD (ii) In the case of GTCCRD < = GPT32n+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF	No transfer
	Up-counting dead time period	No transfer	No transfer
	After up-counting compare match	No transfer	No transfer

Table 23.38 Immediate Double Buffer Transfer from GTCCRD and GTCCRF Registers in Complementary PWM Mode 4

Operation Section	Compare Match State	Immediate Transfer Destination Register		
		GTCCRC	GTCCRE	GTCCRA
Up-counting middle section	Before up-counting compare match	GTCCRD	GTCCRF	(i) In the case of GTCCRF > GPT32n+1.GTCNT GTCCRF (ii) In the case of GTCCRF < = GPT32+1.GTCNT GPT32n+1.GTCNT Negative-phase OFF
	Up-counting dead time period	GTCCRD	GTCCRF	No transfer
	After up-counting compare match	GTCCRD	GTCCRF	No transfer

Table 23.39 Immediate Double Buffer Transfer from GTCCRD and GTCCRF Registers in Complementary PWM Mode 4

Operation Section	Compare Match State	Immediate Transfer Destination Register		
		GTCCRC	GTCCRE	GTCCRA
Down-counting middle section	Before down-counting compare match	GTCCRD	GTCCRF	(i) In the case of GTCCRD < GPT32n.GTCNT GTCCRD (ii) In the case of GTCCRD => GPT32n.GTCNT GPT32n.GTCNT Positive-phase OFF
	Down-counting dead time period	GTCCRD	GTCCRF	No transfer
	After down-counting compare match	GTCCRD	GTCCRF	No transfer

Figure 23.68 to Figure 23.72 show examples of single buffer operation for each operation section in complementary PWM mode 4.

Figure 23.73 to Figure 23.76 show examples of double buffer operation for each operation section in complementary PWM mode 4.

Table 23.40 shows an example for setting complementary PWM mode 4.

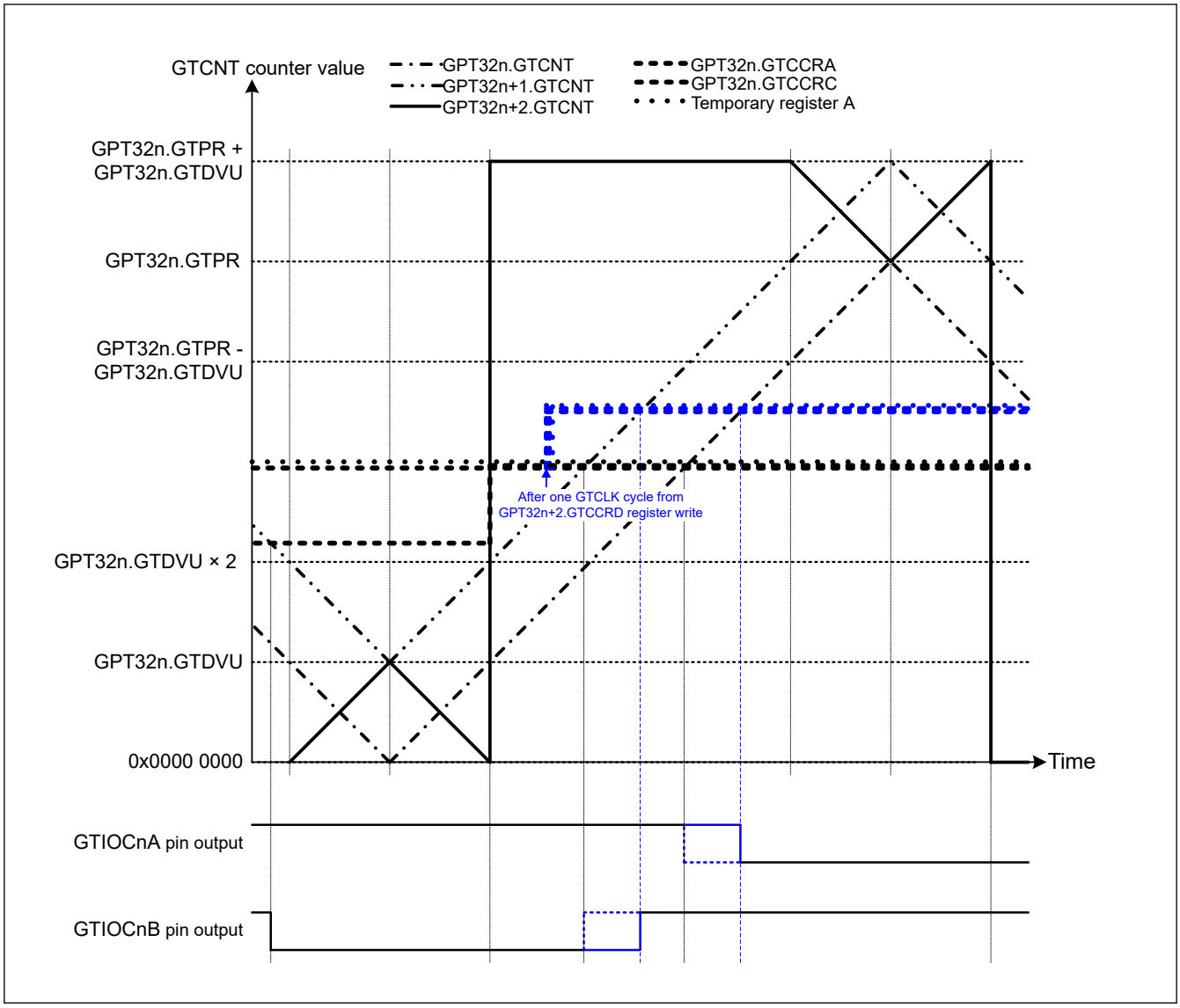


Figure 23.68 **Example of Complementary PWM Mode 4 Single Buffer Operation (Up-Counting Middle Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value larger than the GPT32n+1.GTCNT value is written to GTCCRD register before up-counting compare match) (n = 4, 7)**

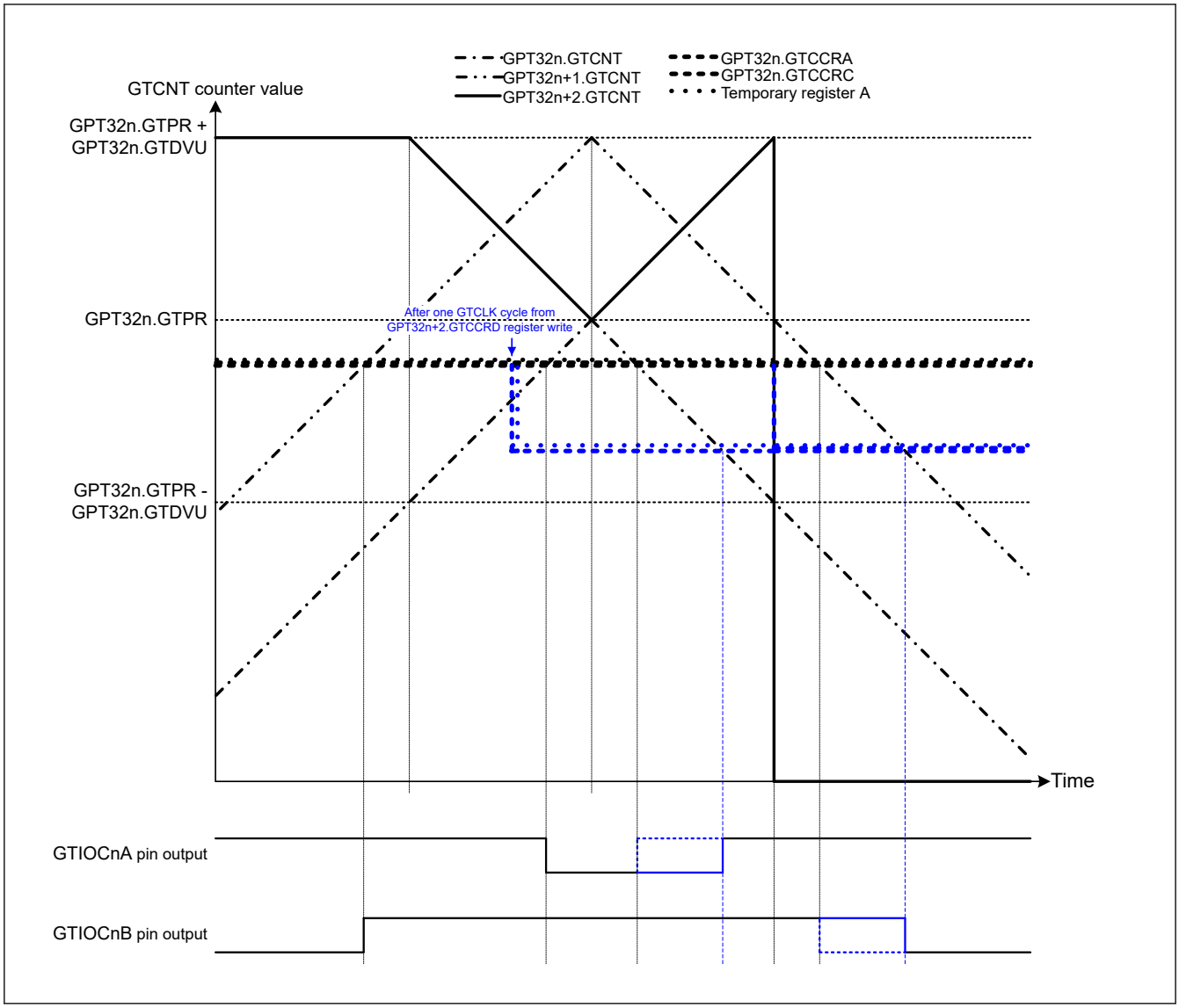


Figure 23.69 **Example of Complementary PWM Mode 4 Single Buffer Operation (Up-Counting Crest Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value is written to GTCCRD register during the up-counting dead time) (n = 4, 7)**

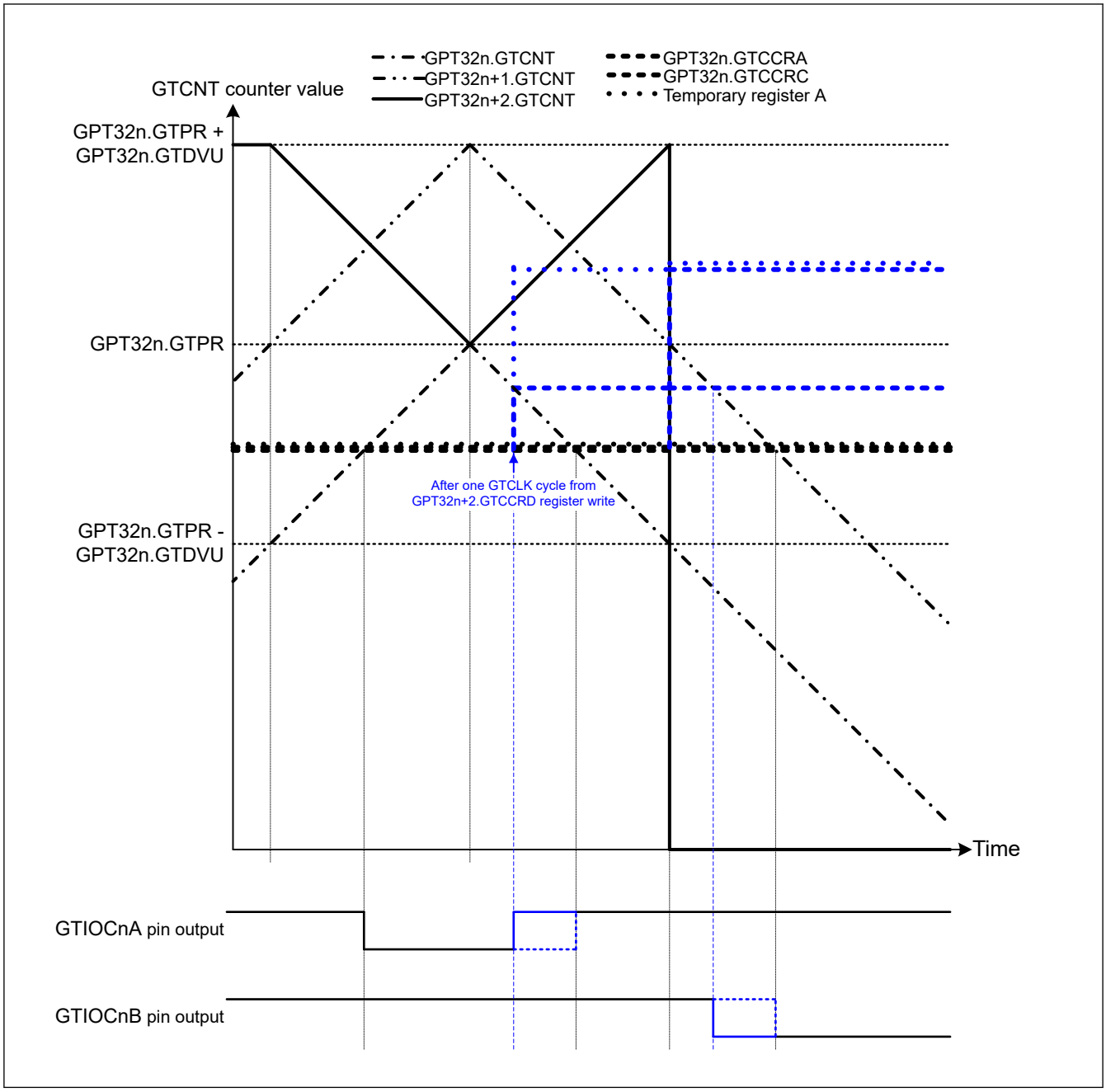


Figure 23.70 Example of Complementary PWM Mode 4 Single Buffer Operation (Down-Counting Crest Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value not less than the GPT32n.GTCNT value is written to GTCCRD register after up-counting compare match before down-counting compare match) (n = 4, 7)

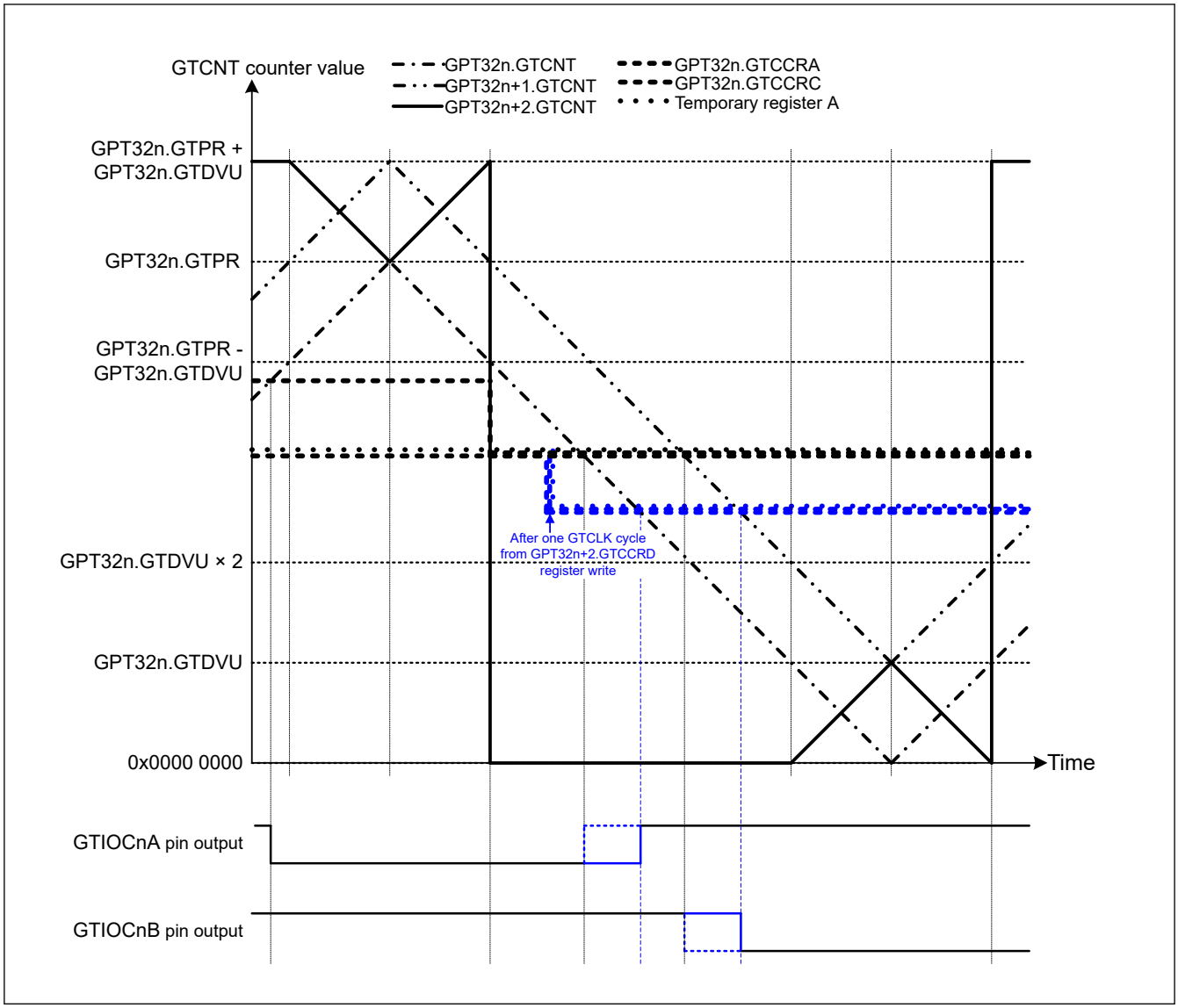


Figure 23.71 **Example of Complementary PWM Mode 4 Single Buffer Operation (Down-Counting Middle Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value smaller than the GPT32n.GTCNT value is written to GTCCRD register before down-counting compare match) (n = 4, 7)**

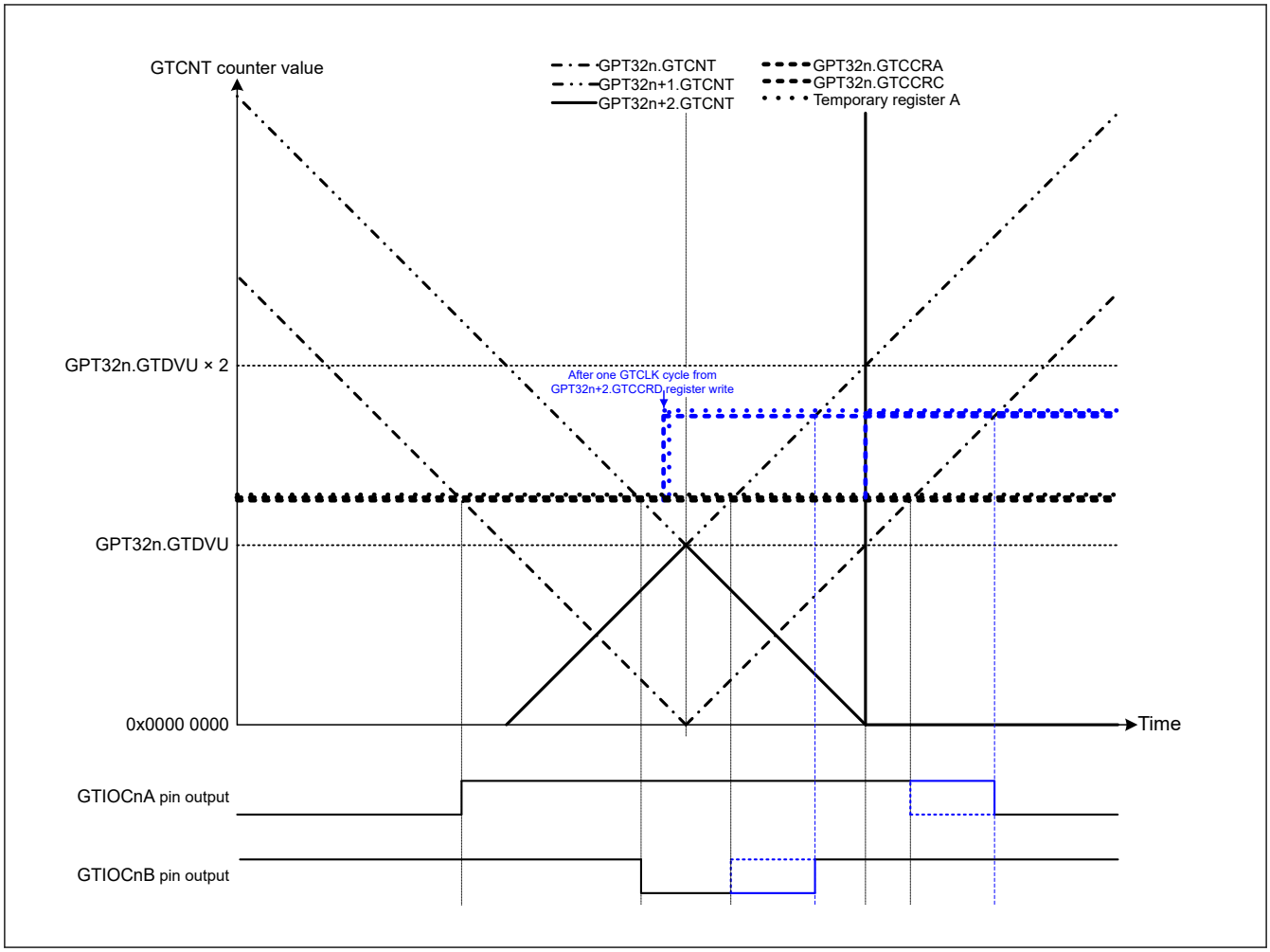


Figure 23.72 **Example of Complementary PWM Mode 4 Single Buffer Operation (Down-Counting Trough Section) (Complementary PWM mode 4 single buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value larger than the GPT32n+2.GTCNT value is written to GTCCRD register after down-counting compare match) (n = 4, 7)**

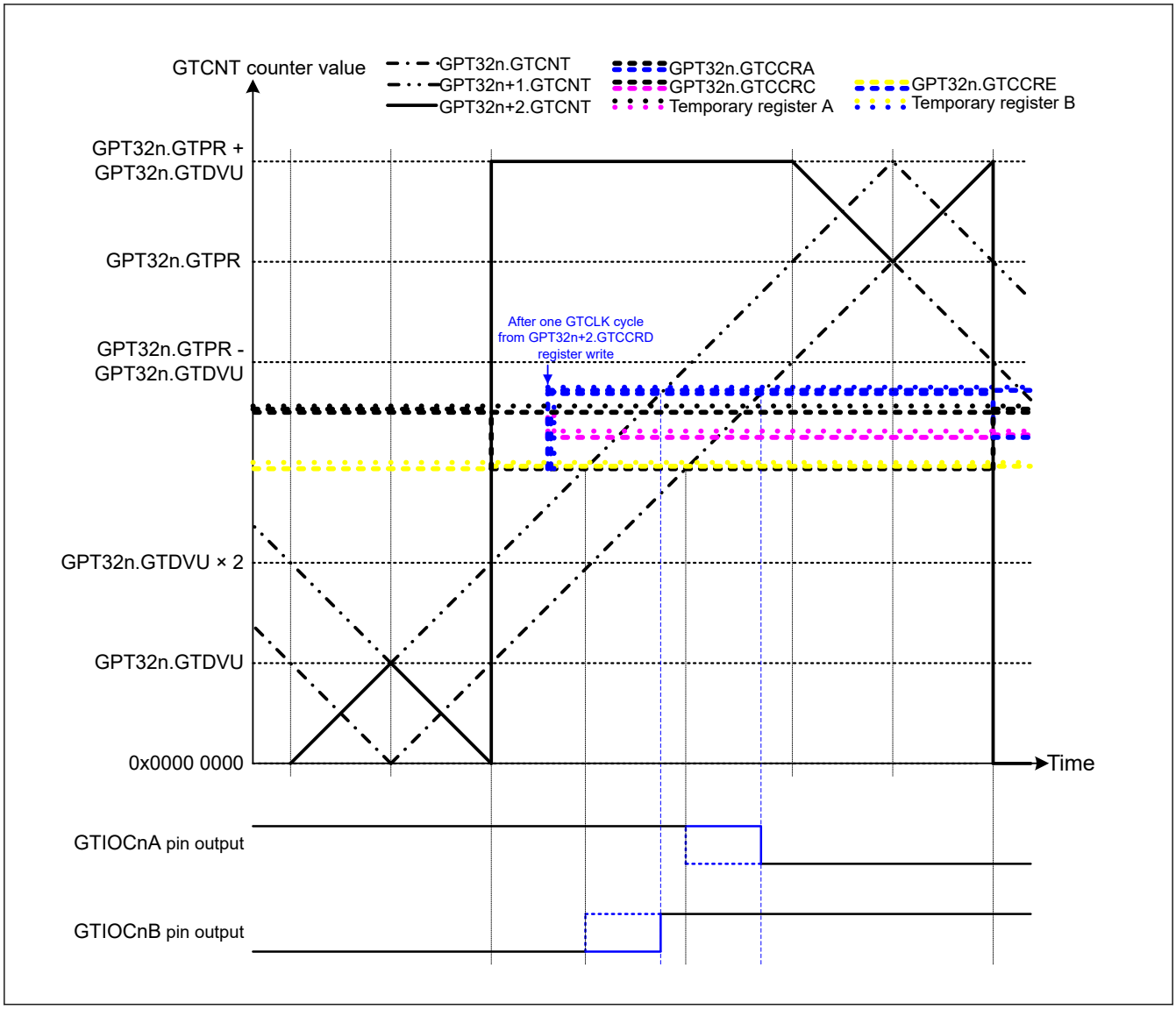


Figure 23.73 **Example of Complementary PWM Mode 4 Double Buffer Operation (Up-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value larger than the GPT32n+1.GTCNT value is written to GTCCRF register before up-counting compare match) (n = 4, 7)**

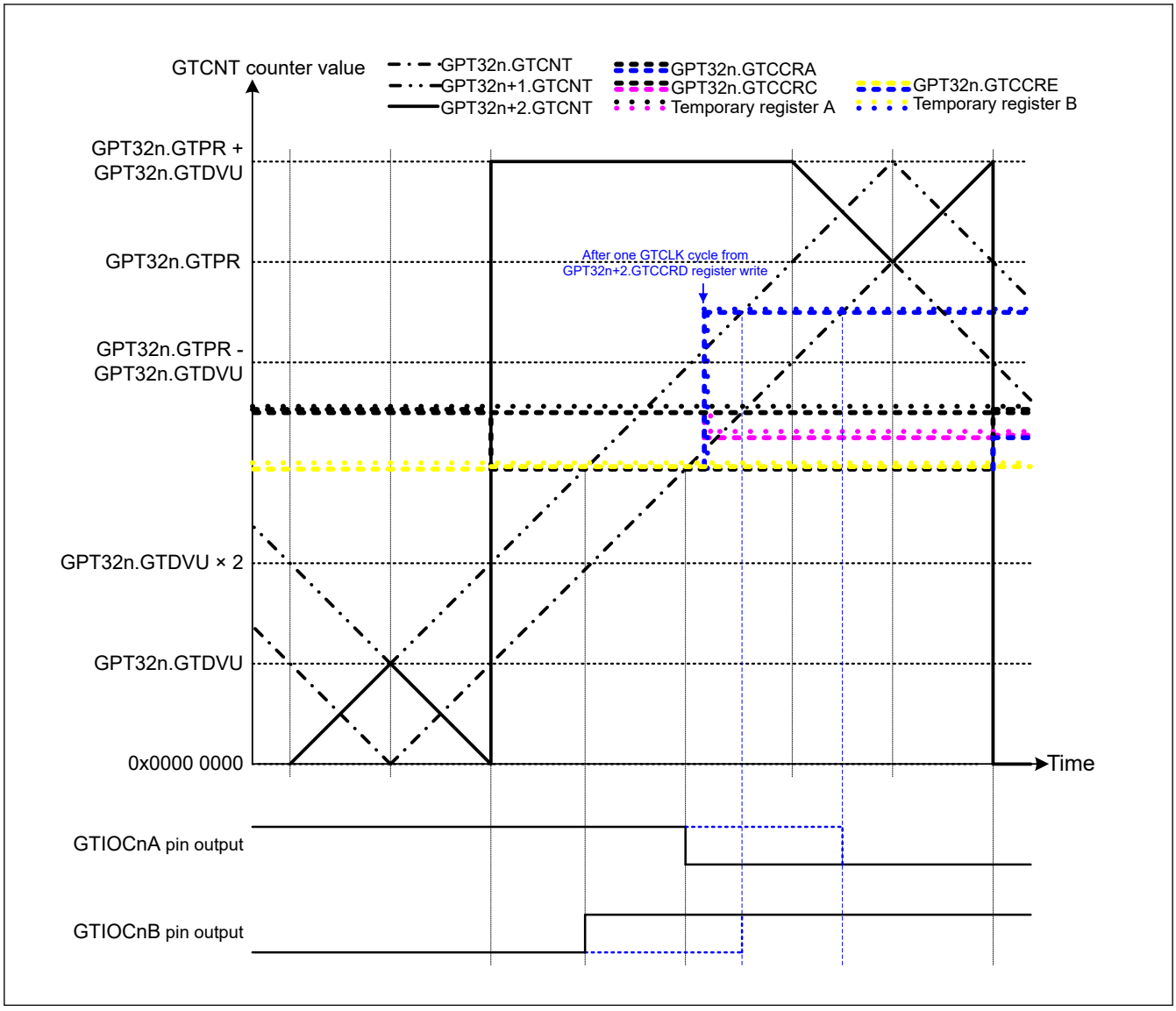


Figure 23.74 **Example of Complementary PWM Mode 4 Double Buffer Operation (Up-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value is written to GTCCRF register after up-counting compare match) (n = 4, 7)**

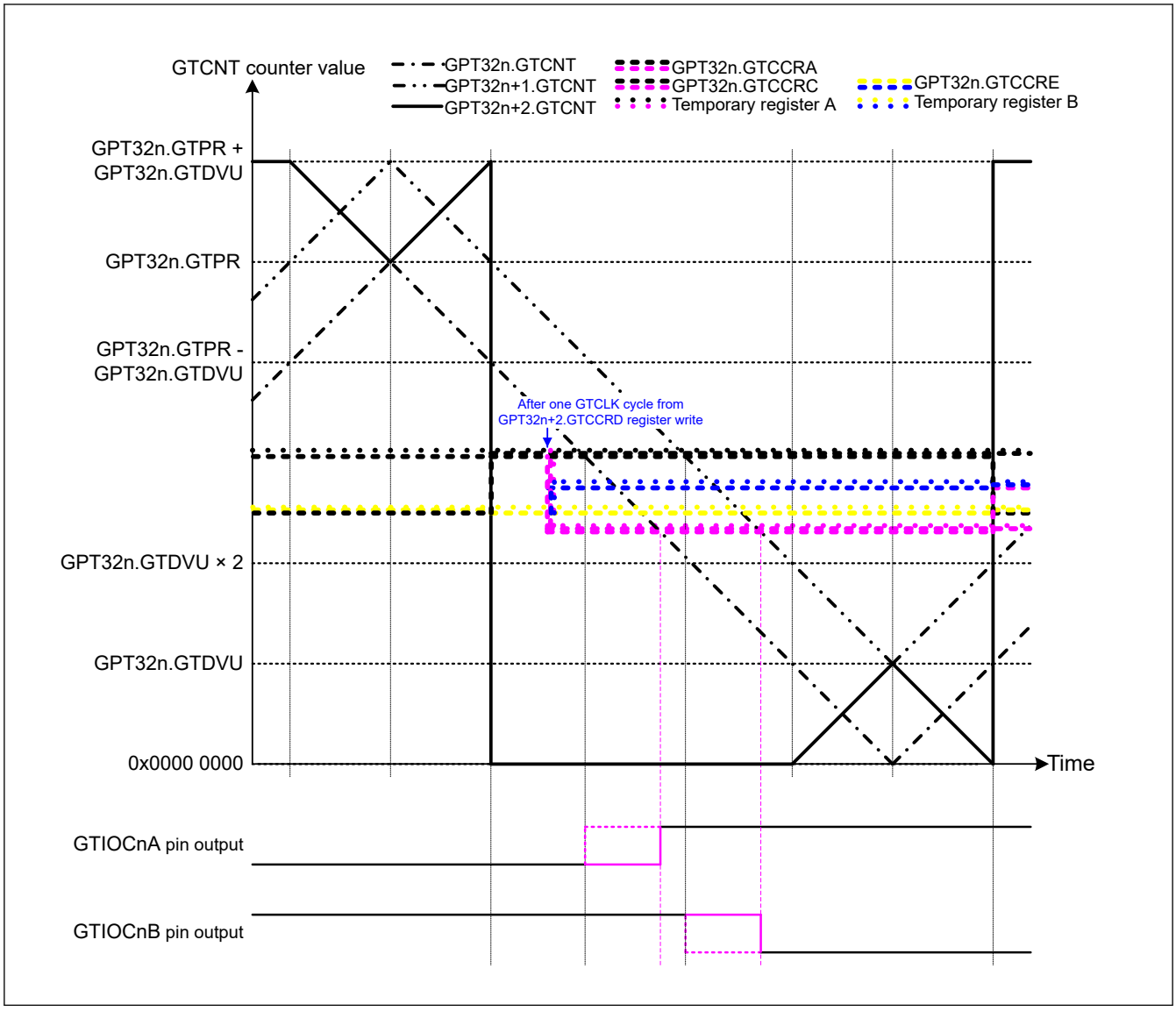


Figure 23.75 **Example of Complementary PWM Mode 4 Double Buffer Operation (Down-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value smaller than the GPT32n.GTCNT value is written to GTCCRD register before down-counting compare match) (n = 4, 7)**

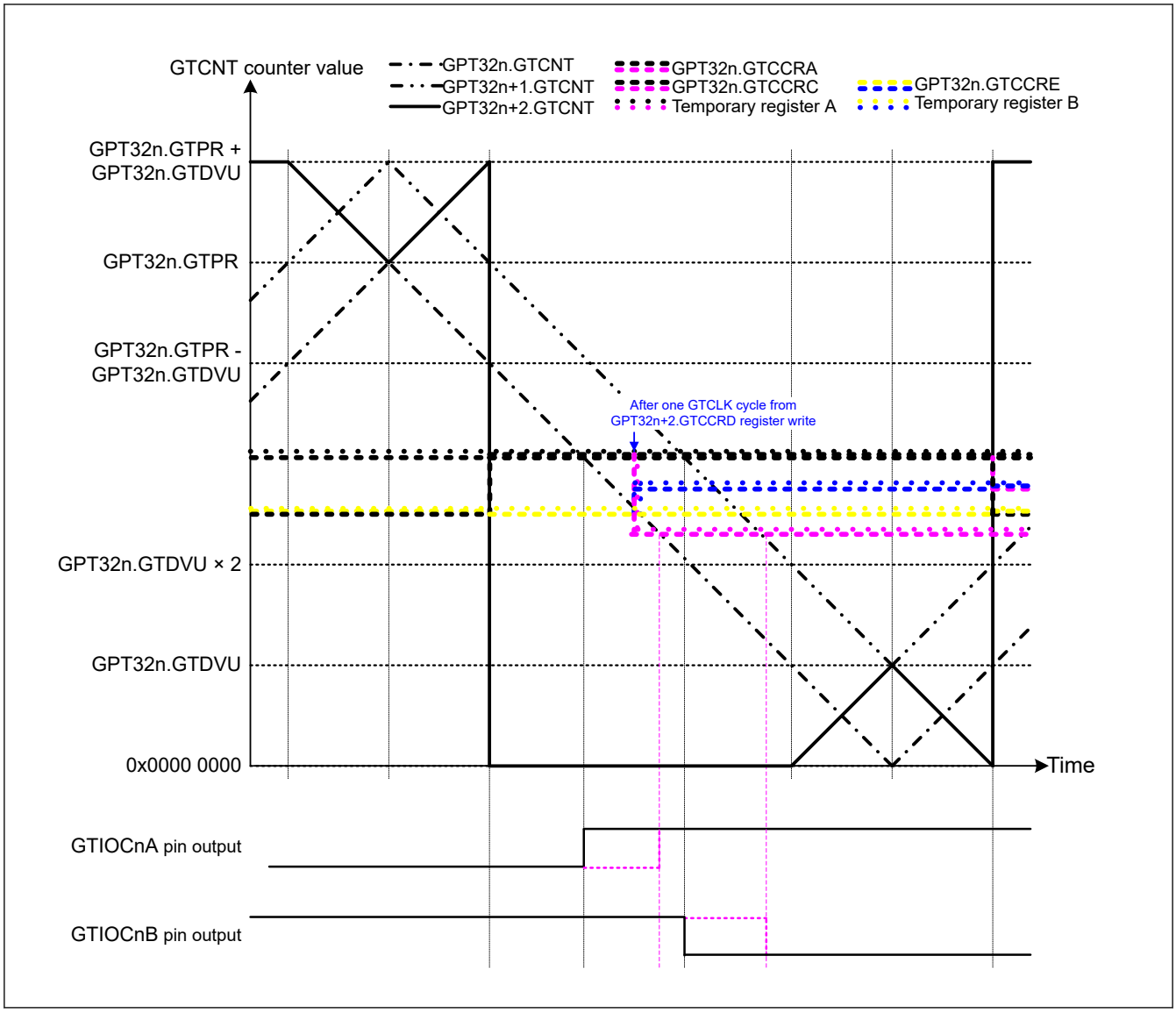


Figure 23.76 **Example of Complementary PWM Mode 4 Double Buffer Operation (Down-Counting Middle Section) (Complementary PWM mode 4 double buffer operation, GTIOCnA pin = Low / GTIOCnB pin = High at GTCCRA register compare match during up-counting, GTIOCnA pin = High / GTIOCnB pin = Low at GTCCRA register compare match during down-counting, when a value is written to GTCCRD register during the down-counting dead time) (n = 4, 7)**

Table 23.40 **Example for Setting Complementary PWM Mode 4 (1 of 2)**

No.	Step Name	Description
1	Set operating mode	Set the operating mode (1111b) with GTCR.MD[3:0] of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in the GPTWn.GTPR, GPTWn.GTPBR and GPTWn.GTPDBR register.
4	Set GTIOCnm /GTIOCn+1m / GTIOCn+2m pin function	Set the function of the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
5	Enable GTCPPOn pin output	Set to enable or disable PWM synchronous output from the GTCPPOn pin with the PSYE bit in the GTIOR register of the GPTWn channel.
6	Enable GTIOCnm / GTIOCn+1m /GTIOCn+2m pin output	Set to enable the output from the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with the OAE and OBE bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
7	Set buffer operation	Set buffer operation with the GTBER2.CP3DB bit of the GPT32n, GPT32n+1, and GPT32n+2 channels.

Table 23.40 Example for Setting Complementary PWM Mode 4 (2 of 2)

No.	Step Name	Description
8	Set compare match value	Set the output pin changing point during up-counting after count start in the GTCCRA register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
9	Set buffer value	For single buffer operation, set data (to be transferred for the first buffer transfer to the GTCCRA register after count start) in the GTCCRD register. For double buffer operation, set data to be transferred at the first end of crest in the GTCCRD register and set data to be transferred at the first end of trough in the GTCCRF register.
10	Set dead time value	Set the dead time value in GTDVU of GTP32n channel.
11	Start count operation	Set GTCR.CST of GPT32n channel to 1 to start count operation.
12	Set compare match value to be transferred immediately	For single buffer operation, set data (to be transferred immediately to the GTCCRA register) in the GTCCRD register. For double buffer operation, set the compare match value for down-counting to be transferred immediately in the GTCCRD register and the compare match value for up-counting in the GTCCRF register. Make settings for the GPT32n+2.GTCCRD register finally. (Data is transferred to the temporary register.)

Note: n = 4, 7
m = A, B

23.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time value (GTDVU and GTDVD value) can automatically be set to GTCCRB.

The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Dead time can be separately set for the first half and second half of a waveform. Dead time for the changing point in the first half of a negative waveform is set in the GTDVU register and that in the second half is set in GTDVD register. The same dead time can also be set for the first and second halves by setting the GTDTCR.TDFER bit to 1.

The GTDBU register can be used as a buffer register of the GTDVU register, and the GTDBD register can be used as a buffer register of the GTDVD registers. Buffer transfer is performed at the end of the cycle (in saw-wave mode: either of an overflow of the GTCNT counter (up-counting), an underflow (down-counting), or the GTCNT counter clearing; in triangle-wave mode: a trough).

The change point of the negative-phase waveform, which is automatically calculated, is obtained by reading the GTCCRB register. Writing to GTCCRB is prohibited when the automatic dead time setting function is used.

Do not set the dead time that makes the change point of the waveform exceeding the count period. When any dead-time setting which would generate a dead-time error is made, adjust the change points of the positive- and negative-phase waveforms to generate waveforms with secured dead-time as shown in Table 23.41. The adjusted change point of the negative-phase waveform is automatically set in the GTCCRB register. An internal signal is used to judge the change point of the positive-phase waveform, thus the value of the GTCCRA register is not updated by the adjusted value.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

In triangle-wave PWM mode, if dead time exceeds the count period by setting 0x00000000 or a value greater than or equal to the setting value of the GTPR register is set in the GTCCRA register, output change is controlled by the output protection function (see section 23.8.4. Output Protection Function for GTIOCnm Pin Output (n = 0 to 13; m = A, B)). When the GTCCRA register is greater than or equal to [GTPR register + GTDVm (m = U, D) register], [GTPR register - 1] is set in the GTCCRB register as the upper limit.

Automatic setting for a dead time value to the GTCCRB register is performed at the next count clock after the register value for calculating the automatic setting value is updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

Table 23.41 Adjustment of the Waveform Change Point When a Dead-Time Error Occurs

PWM Output Operating Mode	Count Direction	Period	Condition for Dead Time Error	Change Point of the Positive-Phase Waveform after Adjustment	Change Point of the Negative-Phase Waveform after Adjustment
Saw-wave one-shot pulse mode	Up-counting	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVD > GTPR (GTCCRA + GTDVU > GTPR)*1	GTPR - GTDVD (GTPR - GTDVU)*1	GTPR
	Down-counting	First half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		Second half	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVD < 0 (GTCCRA - GTDVU < 0)*1	GTDVD (GTDVU)*1	0

Note 1. In the case of GTDTCR.TDFER = 1.

Figure 23.77 to Figure 23.80 show examples of automatic dead time setting function operation. Table 23.42 and Table 23.43 show the setting examples.

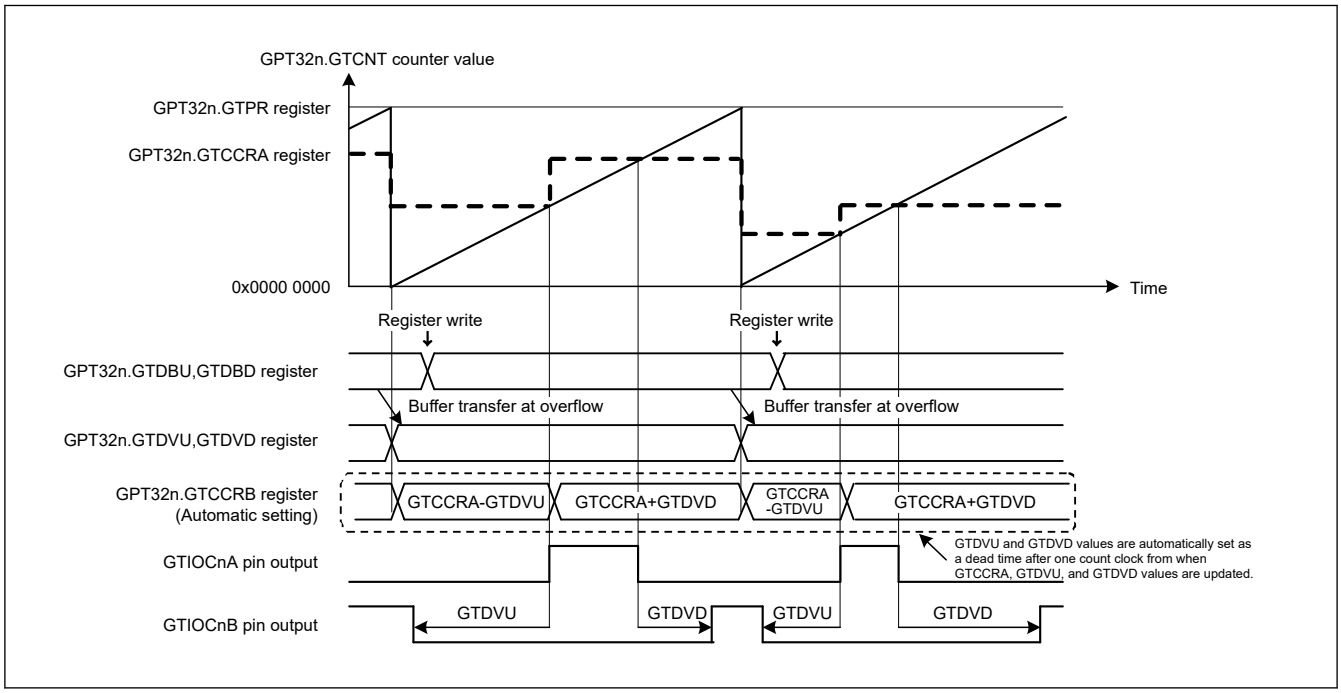


Figure 23.77 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, up-counting, GTDVU and GTDVD set to buffer operation, and active-high

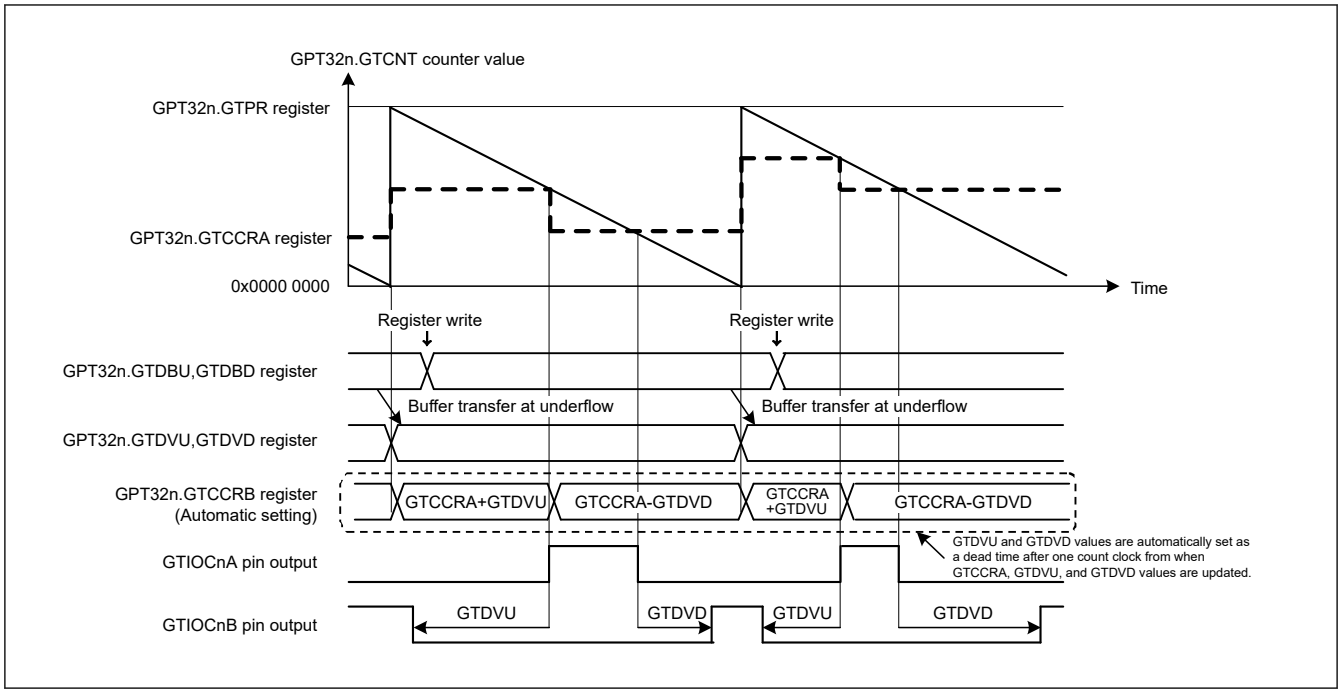


Figure 23.78 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, down-counting, GTDVU and GTDVD set to buffer operation, and active-high

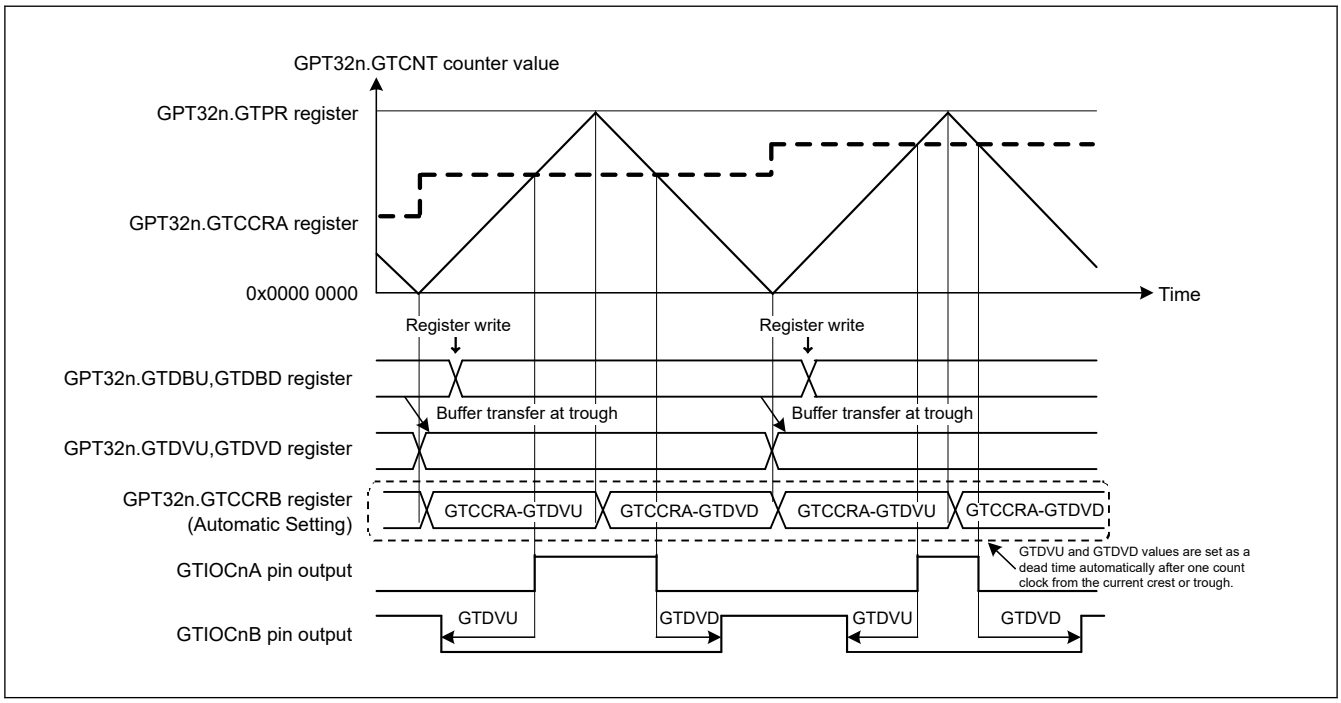


Figure 23.79 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 1, GTDVU and GTDVD set to buffer operation, and active-high

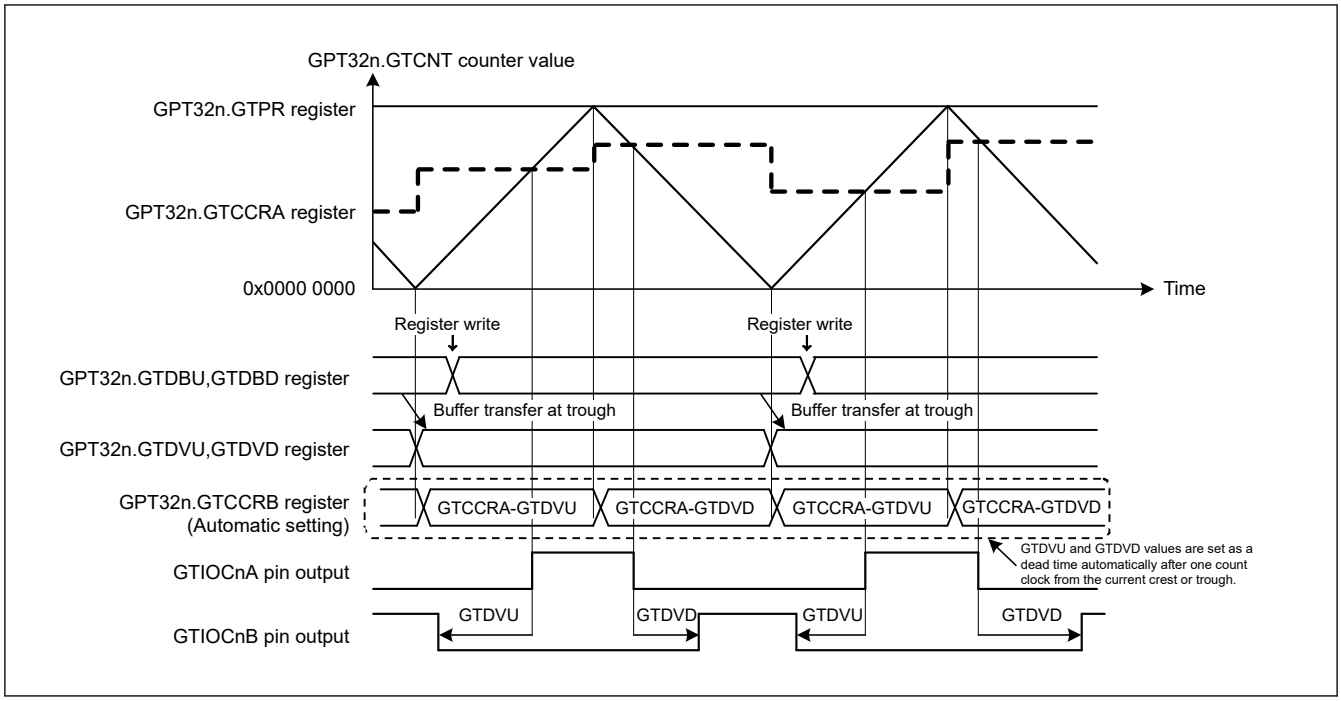


Figure 23.80 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 2 or 3, GTDVU and GTDVD set to buffer operation, and active-high

Table 23.42 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0]. In Figure 23.77 and Figure 23.78, 001b or 0001b (saw-wave one-shot pulse mode) is set. In Figure 23.80, 110b or 0110b (triangle-wave PWM mode 3) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.77, 01b is set after 11b is set in GTUDDTYC[1:0] (up count). In Figure 23.78, 00b is set after 10b is set in GTUDDTYC[1:0] (down count).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 23.77, Figure 23.78, and Figure 23.80, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer value for compare match*1	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD.
9	Set forcible buffer transfer for compare match*1	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly to GTCCRA.
10	Set buffer value for compare match	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD.
11	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
12	Set buffer operation for dead time setting	Set buffer operation with TDBUE and TDBDE bits in GTDTCR.
13	Set dead time value	Set the first half dead time value in GTDVU and the second half dead time in GTDVD. When GTDVU is set with GTDTCR.TDFER bit set to 1, the same value is also set to GTDVD, the same dead time value can be set for the first and second halves.
14	Set buffer value for dead time	For buffer operation, set the first half dead time in one cycle after the current cycle in GTDBU and the second half dead time in GTDBD.

Table 23.42 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
15	Start count operation	Set GTCR.CST to 1 to start count operation.
16	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD. When the dead time register is used for buffer operation, set the dead time value in the first half of the next cycle from the current cycle to GTDBU and the dead time value in the second half to GTDBD.

Note: n: 0 to 13
m: A, B

Note 1. When using PWM Delay Generation circuit, change the order of setting for Enable GTIOCnm pin output and setting for Set buffer value for compare match + Set forcible buffer transfer for compare match.

Table 23.43 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0]. In Figure 23.79, 100b or 0100b (triangle-wave PWM mode 1) is set. In Figure 23.80, 101b or 0101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 23.79 and Figure 23.80, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output*1	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation for compare match	Set buffer operation with CCRA in GTBER.
8	Set compare match value*1	Set the GTIOCnA pin transition in GTCCRA.
9	Set buffer value for compare match	For buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC. For double buffer operation, also set the GTIOCnA pin transition in 2 cycles after the current cycle (in triangle-wave PWM mode 1) or 1 cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRD.
10	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
11	Set buffer operation for dead time setting	Set buffer operation with TDBUE and TDBDE bits in GTDTCR.
12	Set dead time value	Set the first half dead time value in GTDVU and the second half dead time in GTDVD. When GTDVU is set with GTDTCR.TDFER bit set to 1, the same value is also set to GTDVD, the same dead time value can be set for the first and second halves.
13	Set buffer value for dead time	For buffer operation, set the first half dead time in one cycle after the current cycle in GTDBU and the second half dead time in GTDBD.
14	Start count operation	Set GTCR.CST to 1 to start count operation.
15	Set buffer value for each cycle	When the compare match register is used for buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC. When the compare match register is used for double-buffered operation, set the GTIOCnA pin changing point in two cycles after the current cycle (in triangle-wave PWM mode 1) or one cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRD. In the same way, set the dead time value in the first half of the cycle after current cycle in GTDBU and the dead time in the second half in GTDBD.

Note: n: 0 to 13
m: A, B

Note 1. When using PWM Delay Generation circuit, change the order of setting for the GTIOCnm pin output enable and setting for a compare match value.

23.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation stops and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation stops, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change even though the UD bit in GTUDDTYC is modified during the count operation. When the GTUDDTYC.OABDTYT bit is 0, the output duty setting changed when underflow occurs is reflected, and when the GTUDDTYC.OABDTYT bit is 1, the output duty setting changed when underflow occurs and at the top of the triangle-wave is reflected. Similarly, even though the GTUDDTYC.UD bit is modified while the count operation stops and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting and the GTPR value after the start of down-counting is reflected in the count cycle during down-counting.

Figure 23.81 shows an example of count direction changing function operation.

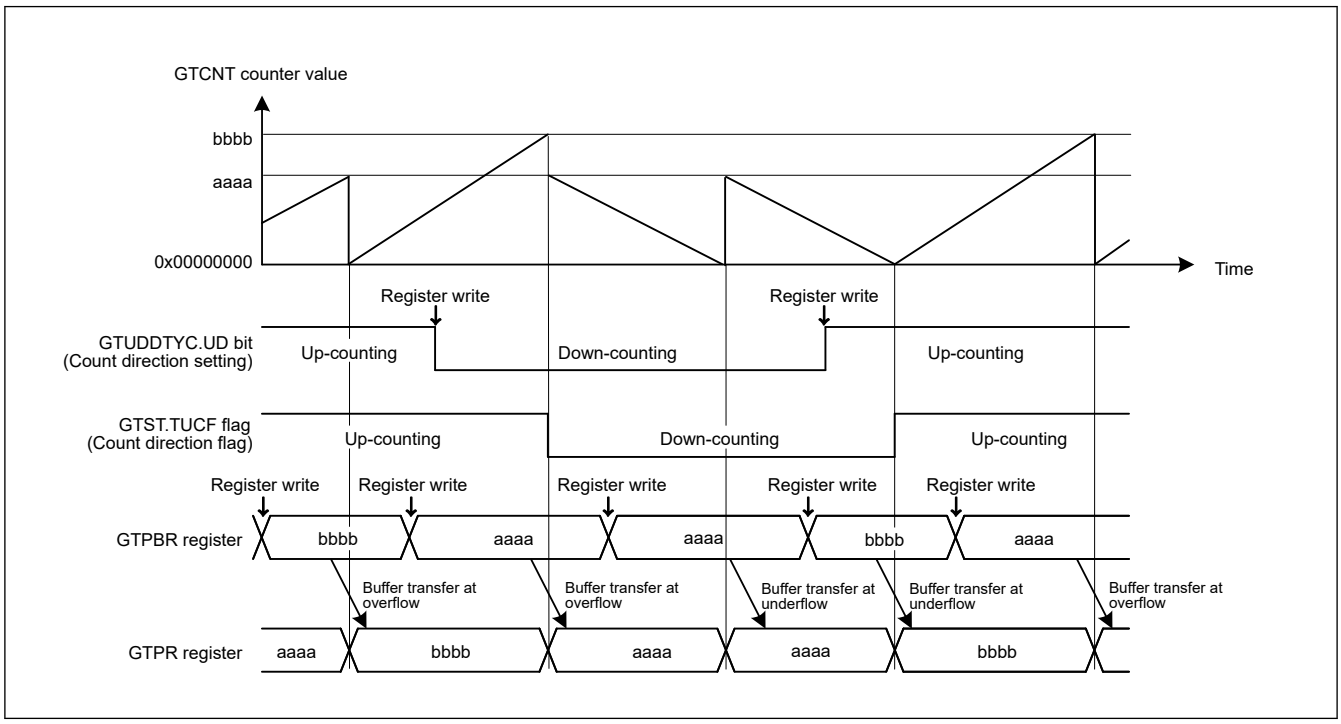


Figure 23.81 Example of a count direction changing function operation during buffer operation

23.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCnA pin and the GTIOCnB pin (n = 0 to 13) are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

This function is invalid in saw-wave PWM mode 2 or complementary PWM mode.

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the

GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, when the GTUDDTYC.OABDTYT bit is 0, the output duty setting changed when underflow occurs is reflected, and when the GTUDDTYC.OABDTYT bit is 1, the output duty setting changed when underflow occurs and at the top of the triangle-wave is reflected.

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation stops and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0% or 100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag
- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCnA pin at cycle end is decided by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCnB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

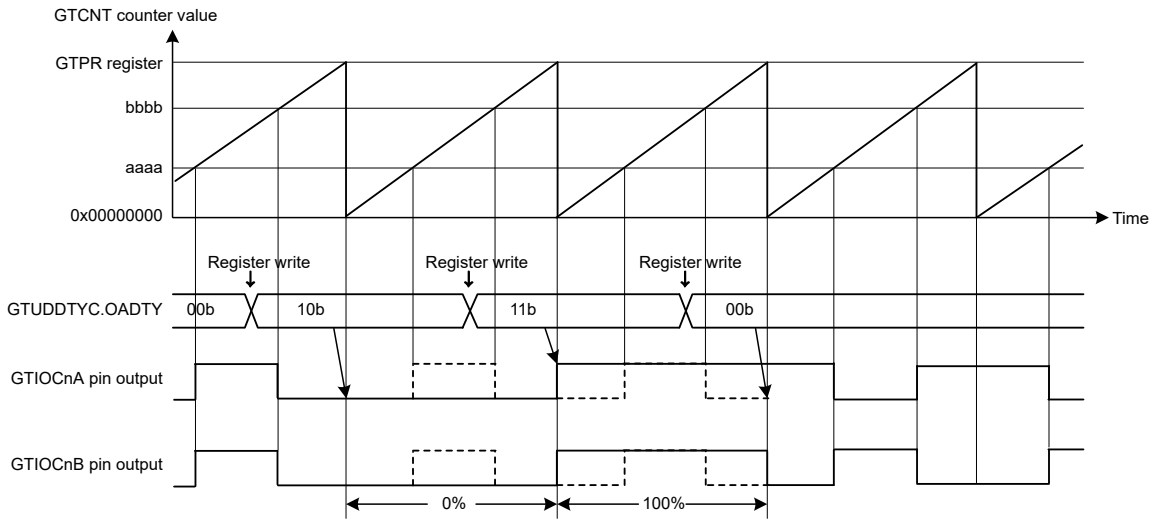
When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 23.44 shows the values of GTIOCnA and GTIOCnB pin output at cycle end.

Table 23.44 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	—	0	0	0	0
10 (high output at cycle end)	—	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 23.82 shows an example of output duty 0% and 100% function.



Note: The base address of registers are the same.

Note: [Setting examples]

GTIOR.GTIOA[4:0] bits:	00011b Initial low output, output toggled at compare match, output retained at cycle end
GTUDDTYC.OADTYR bit:	0b The function selected by GTIOA[3:2] is applied to the output value when the duty cycle is set after release from 0 or 100% duty-cycle setting.
GTIOR.GTIOB[4:0] bits:	00011b Initial low output, output toggled at compare match, output retained at cycle end
GTUDDTYC.OBDTYR bit:	1 The function of GTIOB[3:2] is applied to the compare match output value which is masked after 0 or 100% duty setting release.

Figure 23.82 Example of output duty 0% and 100% function

23.3.7 Hardware Count Start/Count Stop and Clear Operation

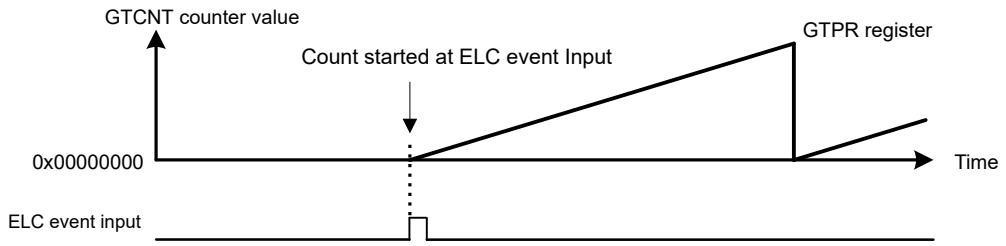
The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCnA and GTIOCnB pin input (n = 0 to 13).

23.3.7.1 Hardware Start Operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 23.83 shows an example of a count start operation by a hardware source. Table 23.45 shows the setting example.



Note: ELC event input: ELCA event input

Figure 23.83 Example of count start operation by a hardware source started at the input of the signal from the ELCA event

Table 23.45 Example setting for count start operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.83, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.83, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 23.83, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in the GTSSR register. In Figure 23.83, GTSSR.SSELCA = 1
7	Set hardware source operation	Set operation of the hardware source selected by the GTSSR register and start counting. In Figure 23.83, the ELCA event input operation is set.

Figure 23.84 shows an example of the timing of operations to start counting in response to ELC_GPTA event input.

This is an example of operations to start counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

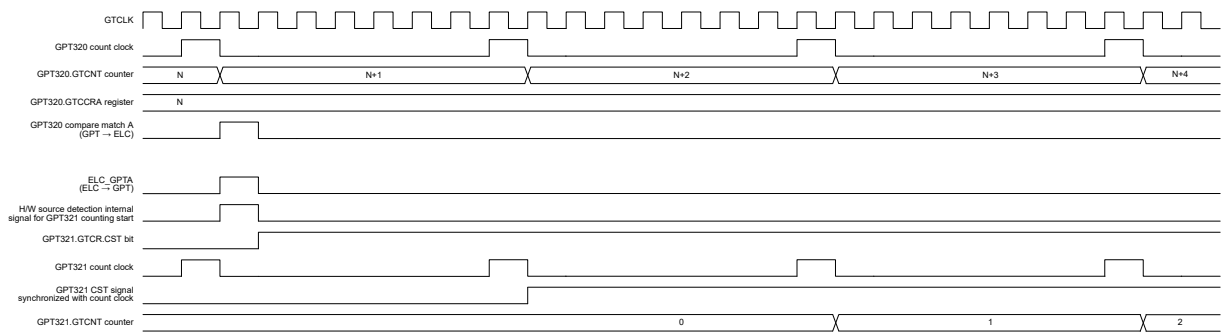
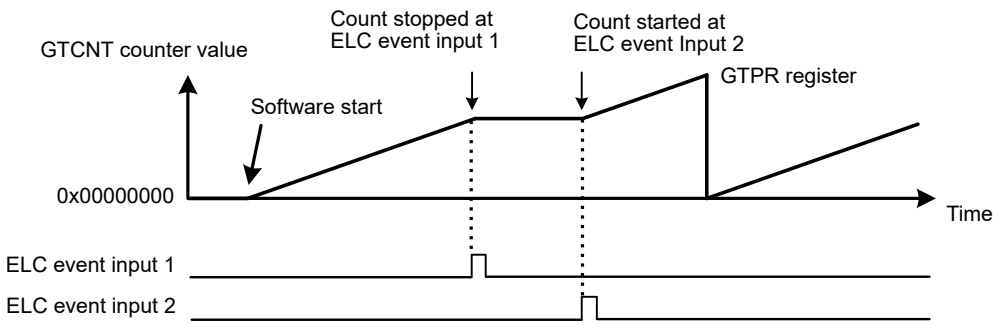


Figure 23.84 Example of Timing of Operations to Start Counting in Response to Event Input from ELC_GPTA

23.3.7.2 Hardware Stop Operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 23.85 shows an example of a count stop operation by a hardware source. Table 23.46 shows the setting example. In this example, the count operation stops at the ELCA event input and restarts at the ELCB event input.



Note: ELC event input 1: ELCA event input
ELC event input 2: ELCB event input

Figure 23.85 Example of count stop operation by hardware source started by software, stopped at ELCA input, and restarted at ELCB input

Table 23.46 Example setting for count stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0] bits. In Figure 23.85, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.85, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 23.85, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register, and wait for count start by the hardware source. In Figure 23.85, GTSSR.SSELCB = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in GTPSR register and wait for count stop by the hardware source. In Figure 23.85, GTPSR.PSELCA = 1.
8	Set hardware source operation	Set operation of the hardware source selected in GTSSR register or GTPSR register, and start or stop counting. In Figure 23.85, ELCA input operation and ELCB input operation are set.

Figure 23.86 shows an example of a count start/stop operation by a hardware source. Table 23.47 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.

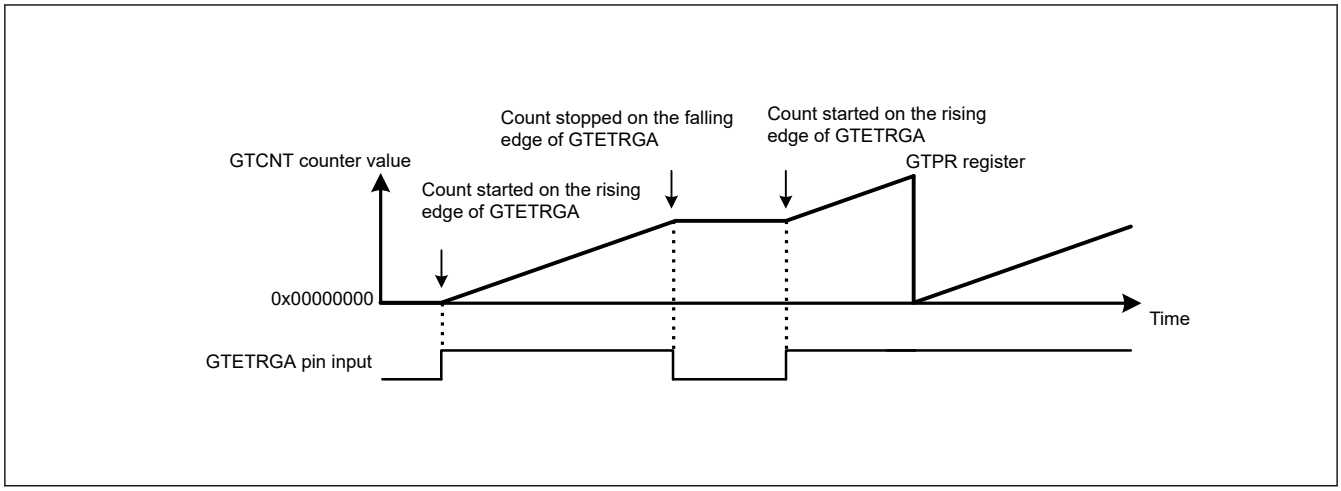


Figure 23.86 Example of count start/stop operation by a hardware source started on the rising edge of GTETRGA pin input, and stopped on the falling edge of GTETRGA pin input

Table 23.47 Example setting for count start/stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.86, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.86, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 23.86, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with the GTSSR register, and wait for count start by the hardware source. In Figure 23.86, GTSSR.SSGTRGAR = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation with the GTPSR register, and wait for count stop by the hardware source. In Figure 23.86, GTPSR.PSGTRGAF = 1.
8	Set hardware source operation	Set operation of the hardware source selected in the GTSSR register or GTPSR register and start or stop counting. In Figure 23.86, the GTETRGA pin operation is set.

Figure 23.87 shows an example of timing of operations to stop counting in response to event input from ELC_GPTA.

This is an example of operations to stop counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

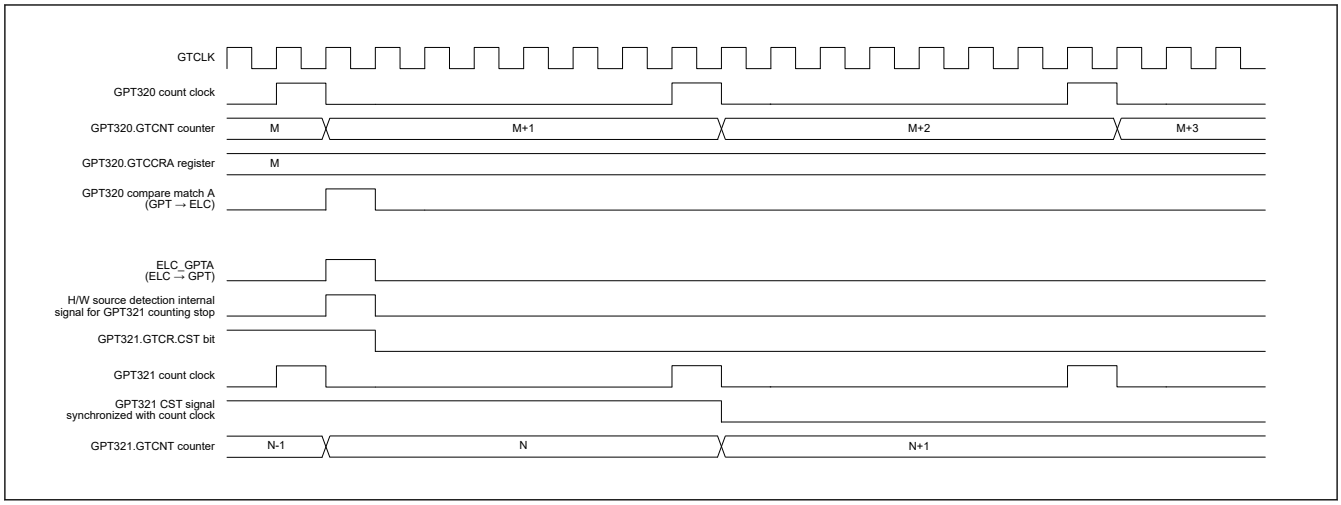


Figure 23.87 Example of Timing of Operations to Stop Counting in Response to Event Input from ELC_GPTA

23.3.7.3 Hardware Clear Operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0 to 13) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 23.88 and Figure 23.89 show examples of the GTCNT counter clearing operation by a hardware source. Table 23.48 shows the setting example. In this example, the GTCNT counter starts at the ELCA input, and the counter stops and clears at the ELCB input.

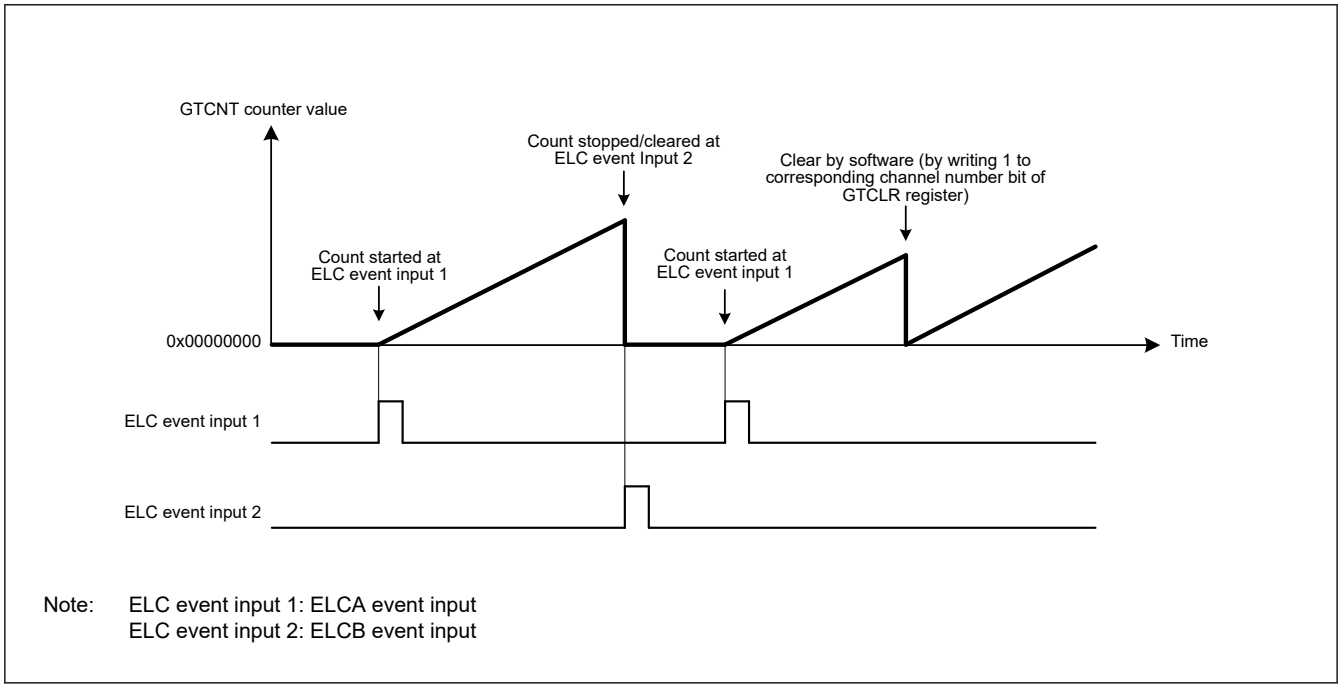
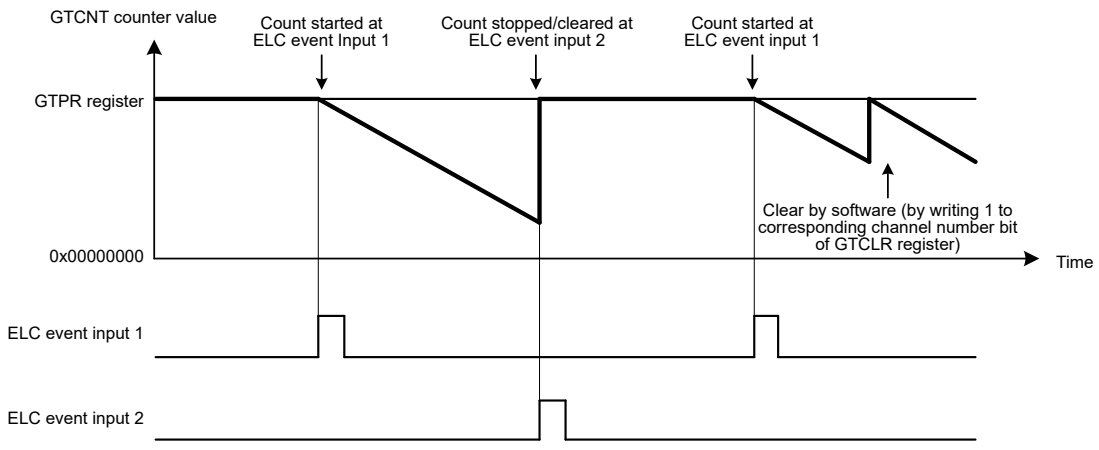


Figure 23.88 Examples of count clearing operation by hardware source in saw wave up-counting, started at ELCA input, and stopped/cleared at ELCB input



Note: ELC event input 1: ELCA event input
ELC event input 2: ELCB event input

Figure 23.89 Examples of count clearing operation by hardware source in saw wave down-counting, started at ELCA input, and stopped/cleared at ELCB input

Table 23.48 Example setting for count clearing operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.88 and Figure 23.89, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.88, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting). In Figure 23.89, after 10b is set in the GTUDDTYC[1:0] bits, 00b is set in the GTUDDTYC[1:0] bits (down-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 23.88, 0x00000000 is set. In Figure 23.89, the GTPR register value is set.
6	Set hardware count start	Select a hardware source for starting count operation in the GTSSR register, and wait for count start by the hardware source. In Figure 23.88 and Figure 23.89, GTSSR.SSELCA = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in the GTPSR register, and wait for count stop by the hardware source. In Figure 23.88 and Figure 23.89, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation in the GTCSR register, and wait for count clear by the hardware source. In Figure 23.88 and Figure 23.89, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in the GTSSR register, GTPSR register or GTCSR register and start, stop or clear counting. In Figure 23.88 and Figure 23.89, the ELCA input and ELCB input are set.

The GPTn_OVF/GPTn_UDF (n = 0 to 13) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 23.90 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 13) interrupt.

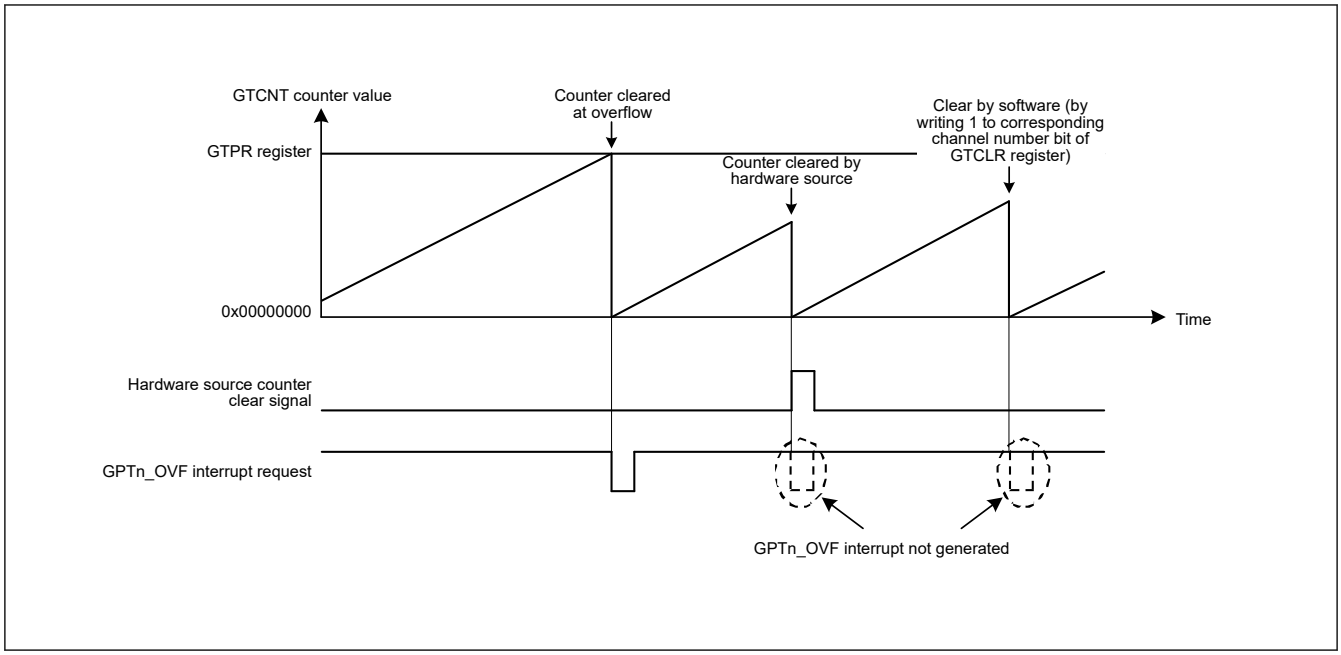


Figure 23.90 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 13) interrupt

Figure 23.91 shows an example of the timing of operations to clear the counter in response to event input from ELC_GPTA when a clock signal produced by frequency-dividing the GTCLK signal is used as the counter clock for the GTCNT counter.

This is an example of operations to clear counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

The GTCNT counter is cleared when counting is in progress after the GPT32 has detected the internal clearing signal.

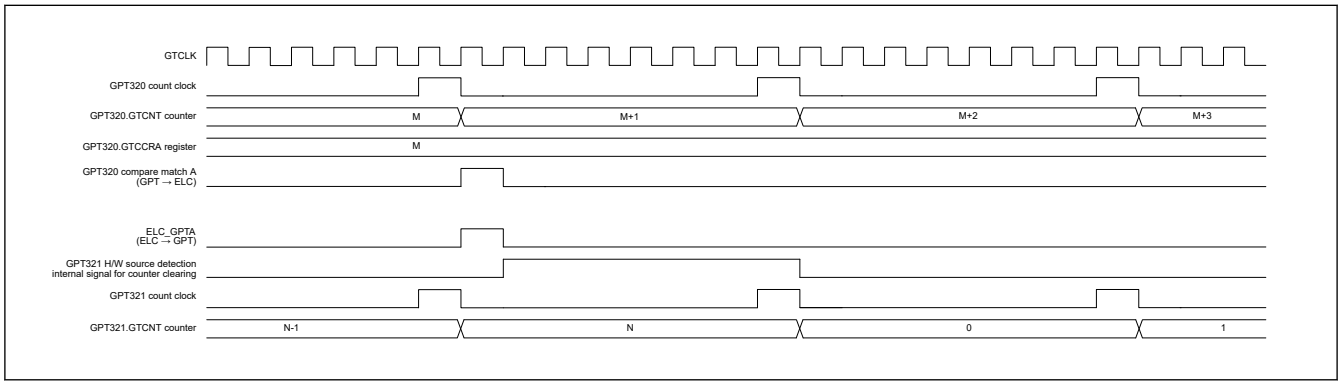


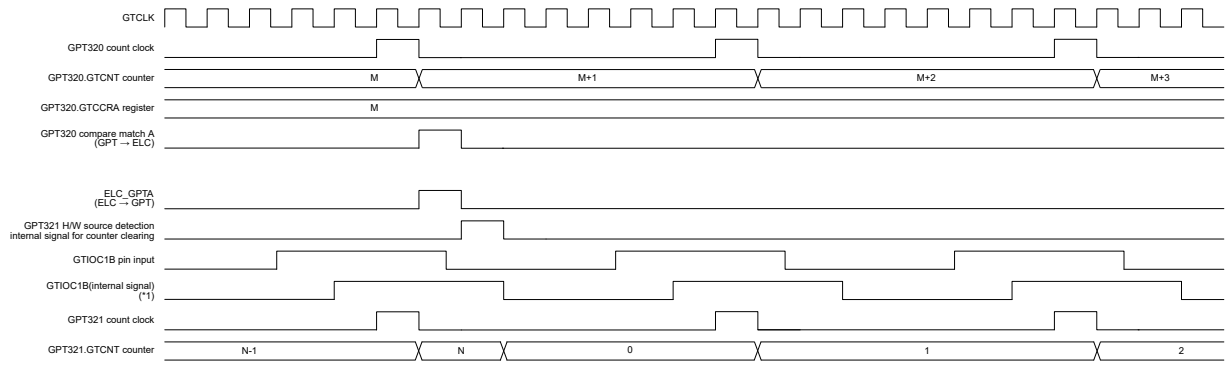
Figure 23.91 Examples of Timing of Operations for Counter Clearing in Response to Event Input from the ELC_GPTA (During the Counting of Cycles of Clock Signal Produced by Dividing the GTCLK Frequency)

Figure 23.92 shows an example of the timing of operations for clearing the counter in response to the input of an event signal from the ELC_GPTA when counting is triggered by a hardware source.

This is an example of operations to clear counting by the GPT321.GTCNT counter in response to a signal. An event signal is output to the ELC after matches in comparison with the GPT320.GTCCRA register. This is selected as a trigger for output to the GPT321 by the ELC as ELC_GPTA.

ELC passes the event signal output from GPT320 without delay to GPT321.

The GTCNT counter is cleared in synchronization with GTCLK after the GPT32 has detected the internal clearing signal.



Note 1. This is the case when the digital noise filter is not in use.

Figure 23.92 Examples of the Timing of Operations for Counter Clearing in Response to Event Input from the ELC_GPTA (During Counting Triggered by Hardware Source)

23.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

23.3.8.1 Synchronized Operation by Software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

When the GTCNT synchronous set/clear function is enabled on the GTCR.SSCEN bit, the GTCNT registers of the channel set in same group on the GTCR.SSCGRP [1:0] bits can be written at the same time.

The synchronous GTCNT write is invalid in complementary PWM mode.

When either the SSCE bit or the SSCD bit of the GTSECR register is set to 1, the GTCR.SSCEN bits of the channels that selected on the GTSECSR register are set to 0 or 1 and the GTCNT synchronous set/clear function of multiple channels are enabled or disabled at the same time.

Because the clock of count operation is selected by GTCR.TPCS[3:0] bits in respective channels, if the clock period of each channel that performs synchronous operation (count start/stop/clear) is different from others, the synchronous operation timings of every channel are not exact same.

Figure 23.93 shows an example of a simultaneous start, stop, and clear by software. Figure 23.94 shows an example of phase start operation by software. Figure 23.95, Figure 23.96, Figure 23.97 show an example of simultaneous start/stop/clearing with different count period.

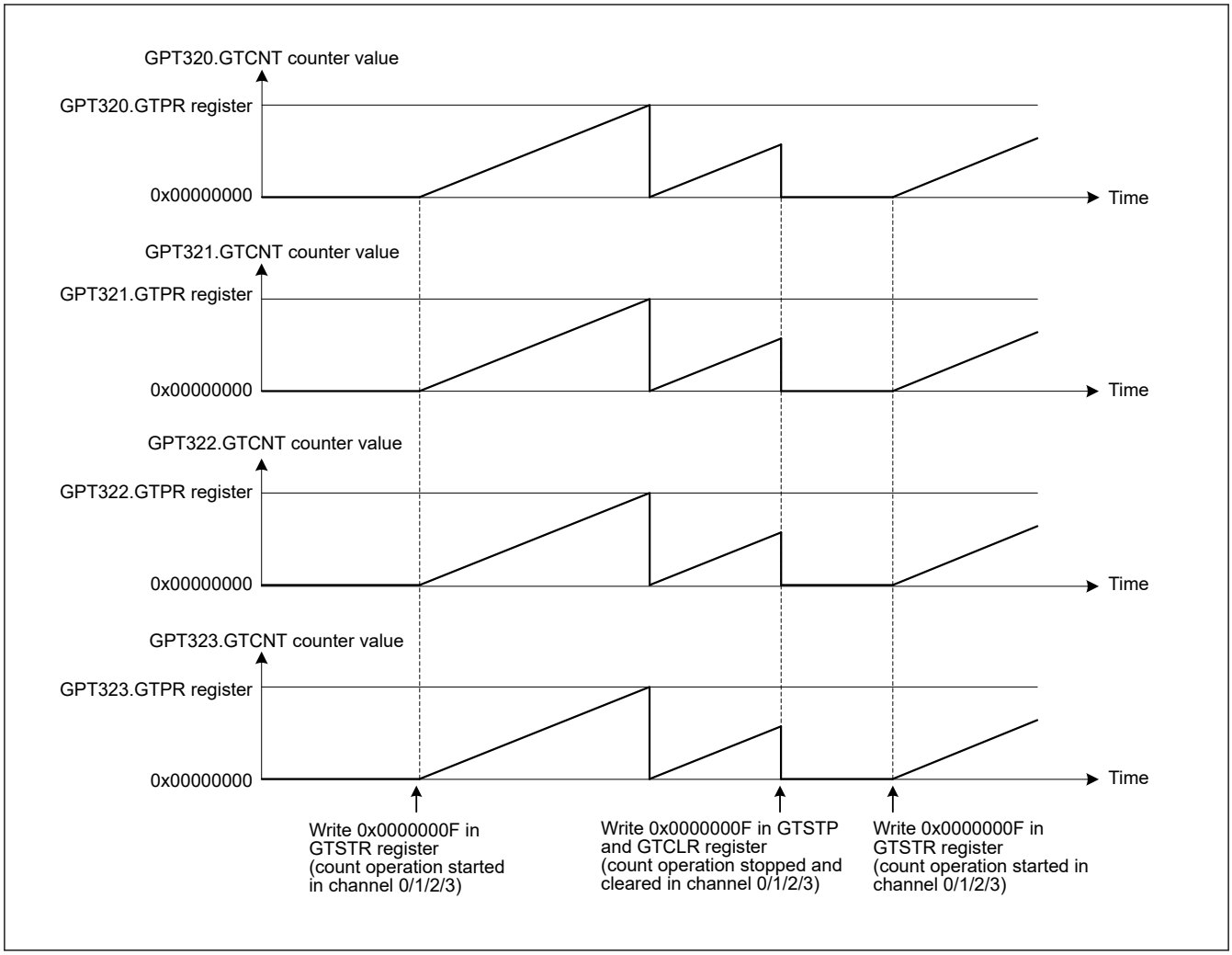


Figure 23.93 Example of a simultaneous start, stop, and clear by software with the same count cycle (GTPR register value)

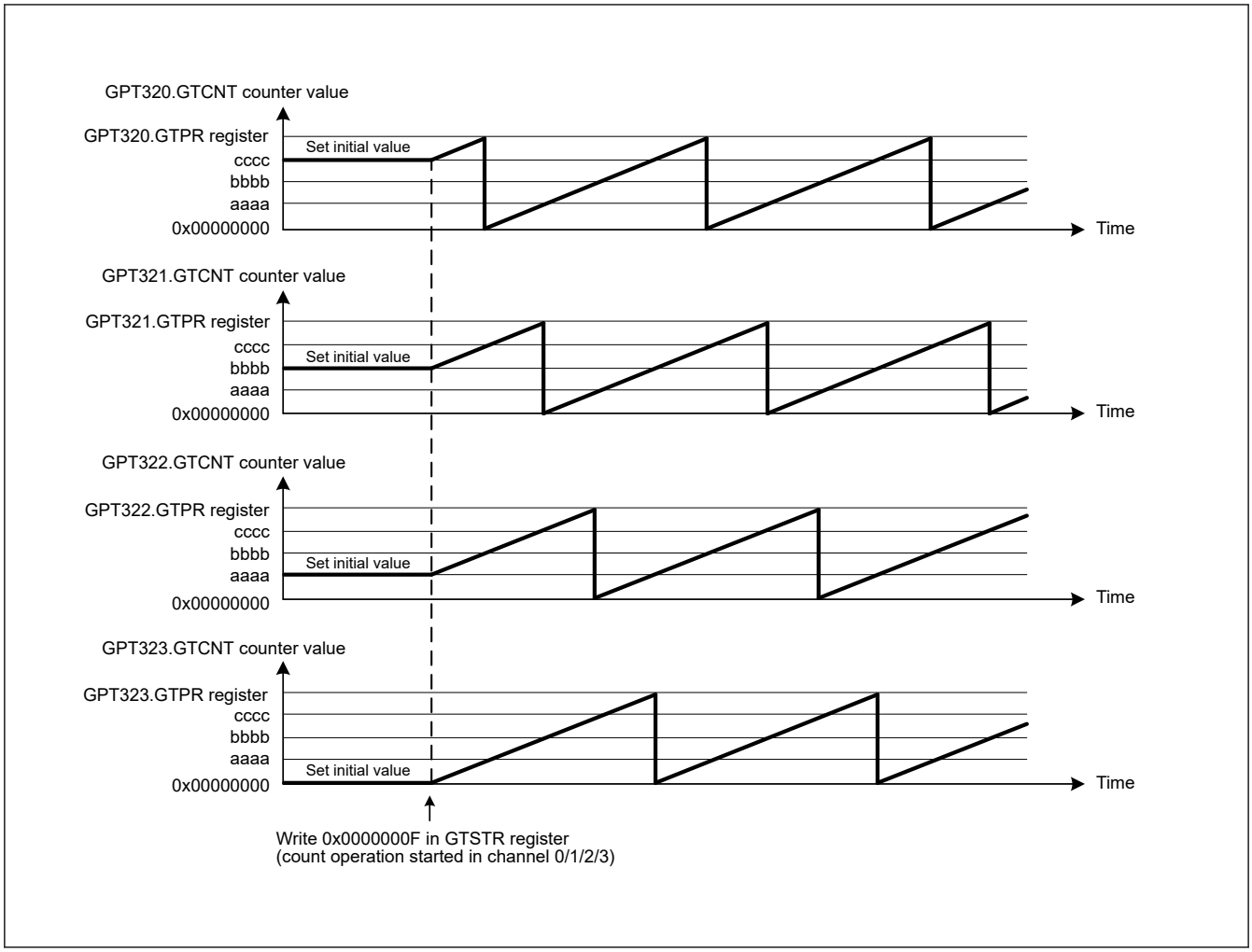


Figure 23.94 Example of software phase start with the same count cycle (GTPR register value)

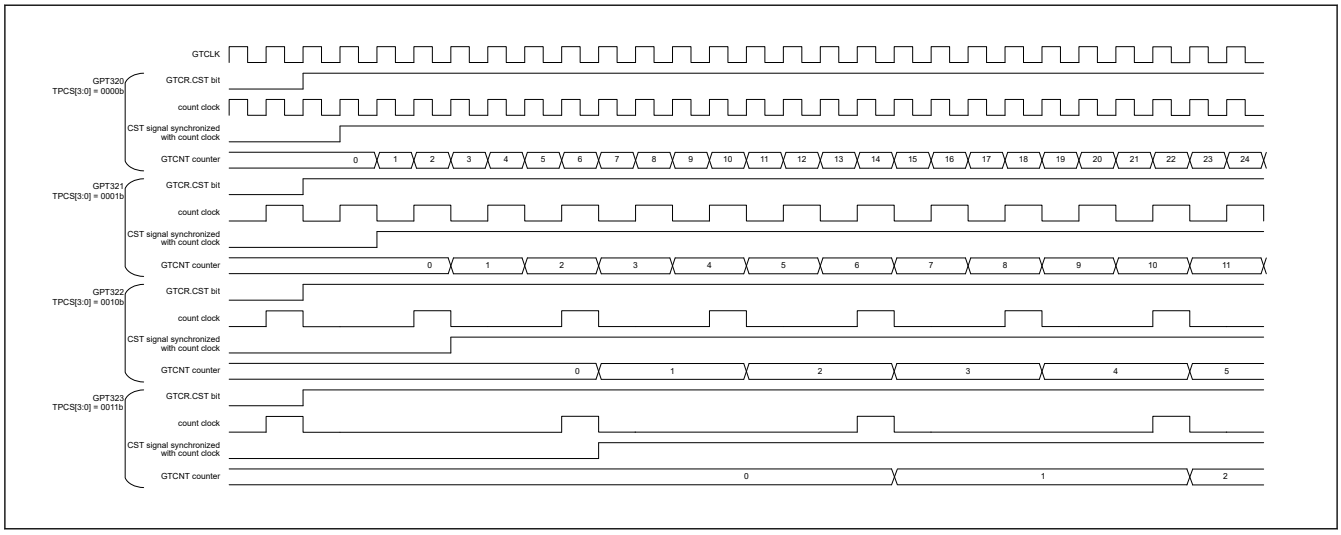


Figure 23.95 Example of Simultaneous Start Operation by Software (with Different Count Period)

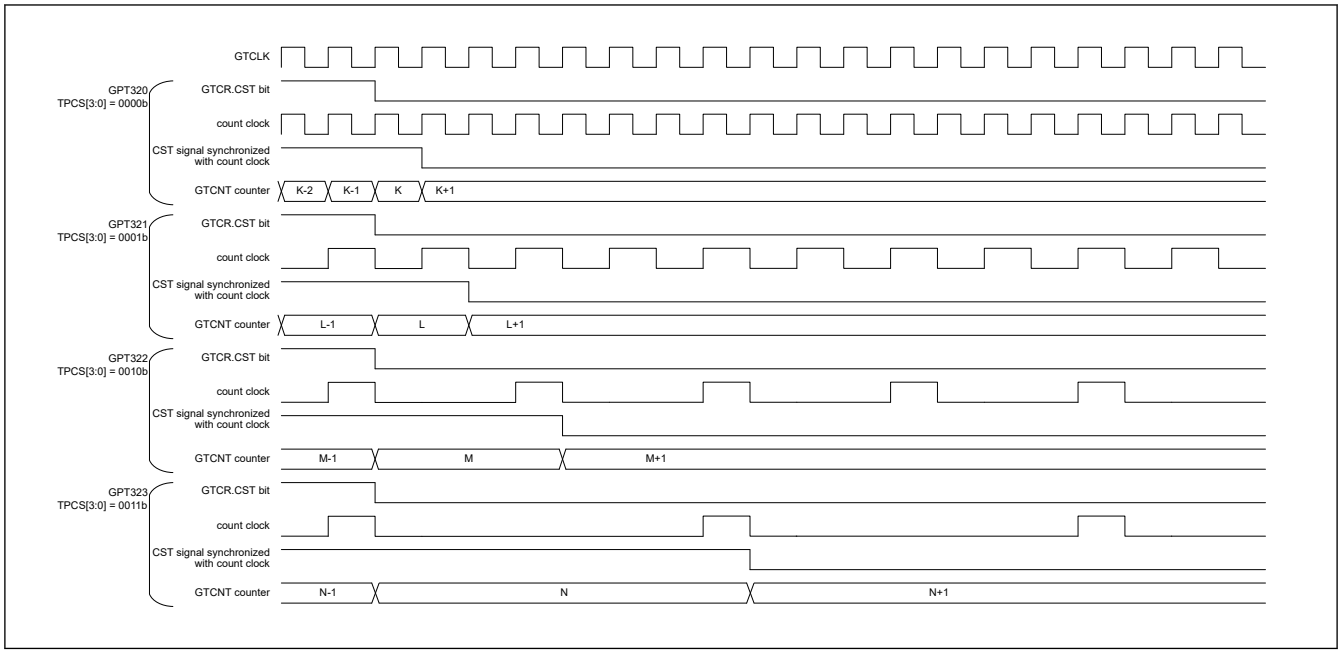


Figure 23.96 Example of Simultaneous Stop Operation by Software (with Different Count Period)

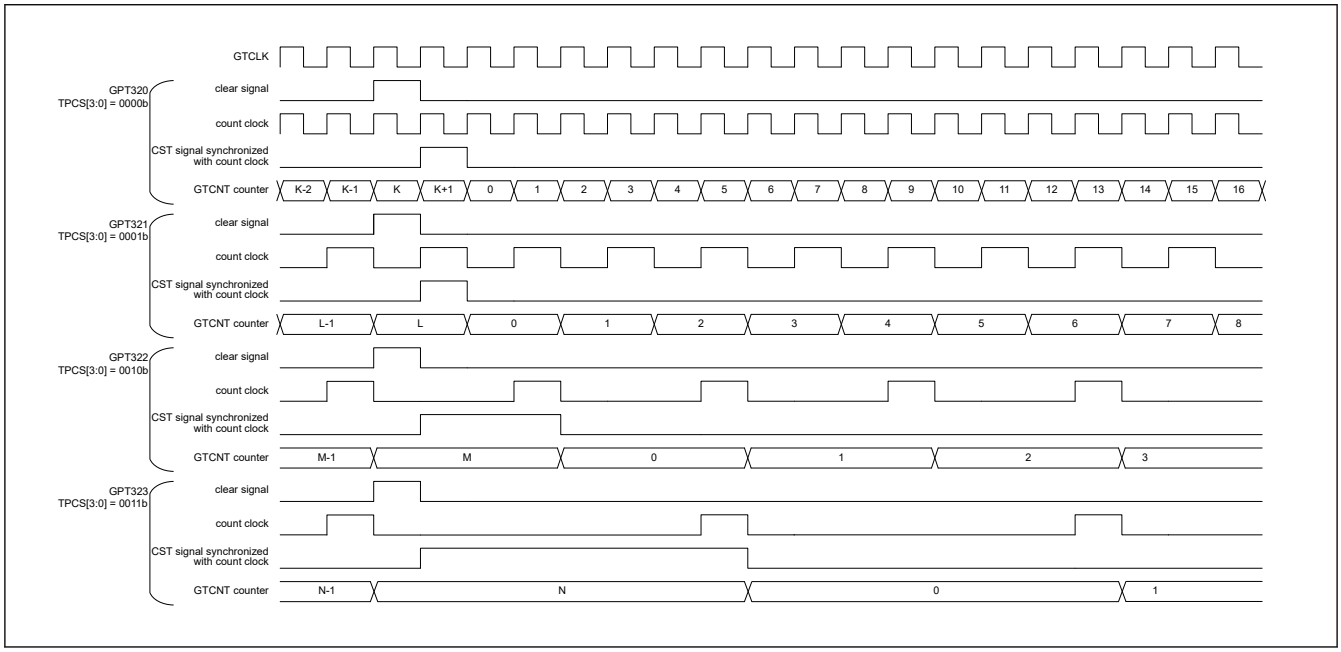
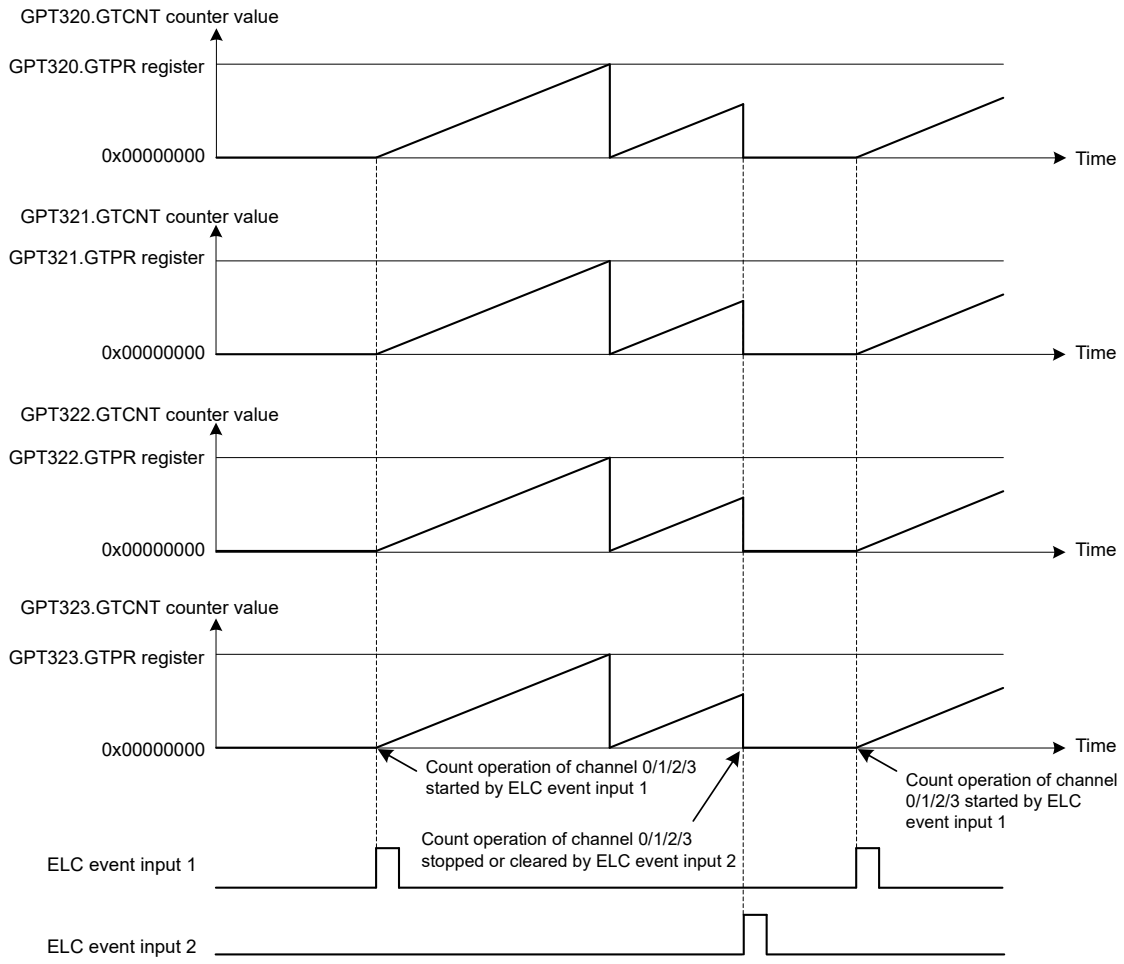


Figure 23.97 Example of Simultaneous Clearing Operation by Software (with Different Count Period)

23.3.8.2 Synchronized Operation by Hardware

The counters for multiple channels can be started, stopped, and cleared simultaneously by ELC event input.

Figure 23.98 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Table 23.49 shows the setting example.



Note: ELC event input 1: ELCA event input
ELC event input 2: ELCB event input

Figure 23.98 Example of a simultaneous start, stop, and clear by a hardware source with the same count cycle (GTPR register value)

Table 23.49 Example setting for simultaneous start by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.98, 000b or 0000b (saw-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.98, after 11b is set in the GTUDDTYC[1:0] bits, 01b is set in the GTUDDTYC[1:0] bits (up-counting).
3	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 23.98, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with the GTSSR register, and wait for count start by the hardware source. In Figure 23.98, GTSSR.SSELCA = 1.

Table 23.49 Example setting for simultaneous start by a hardware source (2 of 2)

No.	Step Name	Description
7	Set hardware count stop	Select a hardware source for stopping count operation with the GTPSR register, and wait for count stop by the hardware source. In Figure 23.98, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation with the GTCSR register, and wait for count clear by the hardware source. In Figure 23.98, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in the GTSSR, GTPSR, or GTCSR registers, and start, stop, or clear counting. In Figure 23.98, ELCA input and ELCB input are set.

23.3.8.3 Input Capture Operation by Inter Channel Cooperation

The events of compare match, input capture, sawtooth wave up-count overflow, sawtooth wave down-count underflow, the crest and trough of triangle wave and complementary PWM mode and the count clock can be used as the input capture factor for the GTCCRm register (m = A or B) of other channels. The input capture factors by inter channel cooperation can be set by the GTICCR register of the channel that generates the input capture factor. Input capture by other channel factors can be enabled by GTICmSR.mSOC bit (m = A or B) in the captured channels. The channels that generate input capture factors and the channels that are captured are set to the same input capture group by GTICCR.ICmGRP[1:0] bits (m = A or B).

Figure 23.99 shows an example of input capture operation by inter channel cooperation and Table 23.50 shows an example for setting input capture operation by inter channel cooperation.

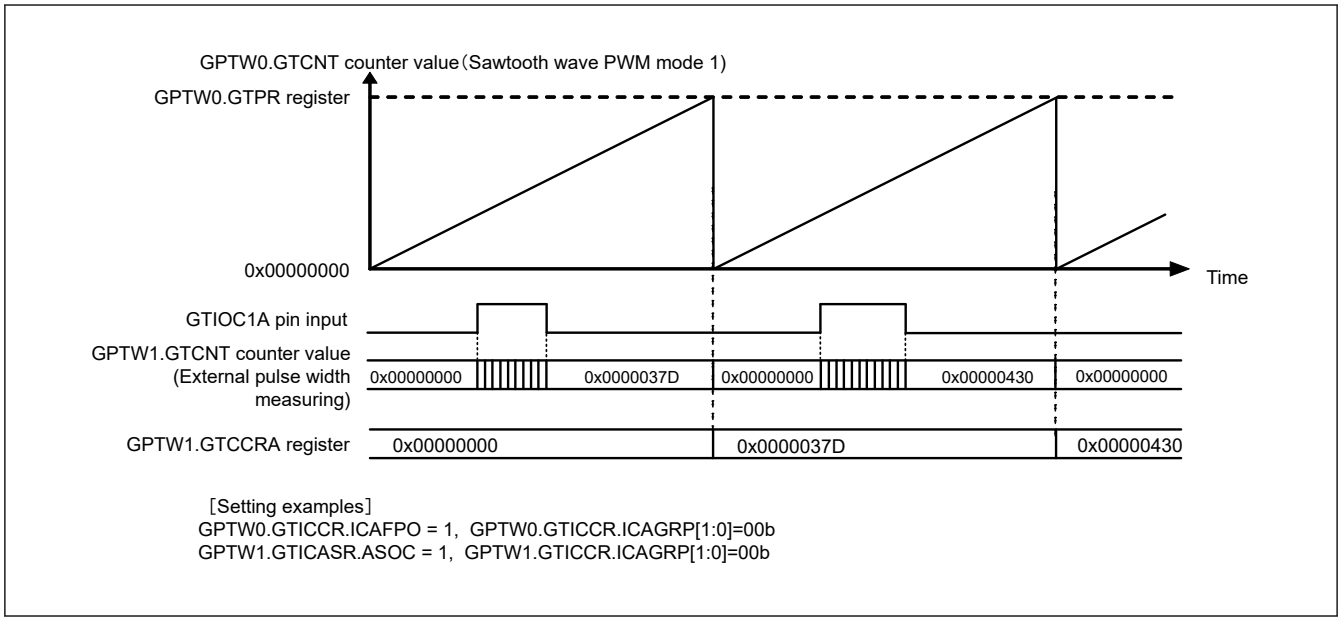


Figure 23.99 Example of input capture operation by inter channel cooperation (channel 1 is captured by the overflow of channel 0)

Table 23.50 Example for setting input capture operation by inter channel cooperation (1 of 2)

Step name	Description
(1) Set operating mode	Set the operating mode with the GTCR.MD[2:0] or the GTCR.MD [3:0] bits. In Figure 23.99,GTCR.MD[2:0] = 000b or GTCR.MD[3:0] = 0000b (sawtooth-wave PWM mode 1) is set to GPTW0.

Table 23.50 Example for setting input capture operation by inter channel cooperation (2 of 2)

Step name	Description
(2) Set external pulse width measuring function	Enable external pulse width measuring function with the GTUPSR.USILVL [3: 0] bits for up-counting operation and the GTDNSR.DSILVL [3: 0] bits for down-counting operation and select the input pin and level to measure. In Figure 23.99, GTUPSR.USILVL[3:0] = 0011b (count up when GTIOCnA pin is 1).
(3) Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 23.99, for GPTW0, lower 2 bits of the GTUDDTYC register is set to 11b, and then lower 2 bits of the GTUDDTYC register is set to 01b (up-counting).
(4) Select count clock	Select the count clock with GTCR.TPCS[2:0] bits or GTCR.TPCS [3:0] bits of the corresponding channel.
(5) Period setting	Set a period in the GTPR register of the corresponding channel.
(6) Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel.
(7) Set counter clear factor to the inter channel cooperation Input capture (cleared channels)	Set the GTCSR.CSCMSC[2:0] bits in the channel to be cleared by input capture by inter channel cooperation to 001b, 010b, and select input capture as counter clear factor. In Figure 23.99, GPTW1.GTCSR.CSCMSC[2:0] bits are 001b.
(8) Inter channel cooperation input capture setting (source channel)	Set the input capture factor using the GTICCR register in the source channels of inter channel cooperation input capture. In Figure 23.99, GPTW0.GTICCR.ICAFPO bit is 1b.
(9) Inter channel cooperation input capture setting (captured channels)	Set the GTICmSR.mSOC bit (m = A or B) in the captured channels to allow input capture to the GTCCRm register (m = A or B) by other channel factors. In Figure 23.99, GPTW1.GTICASR.ASOC bit is 1b.
(10) Set group of inter channel cooperation input capture	Set the same value to the GTICCR.ICmGRP[1:0] bits (m = A or B) in the source channels and cleared channels of inter channel cooperation input capture and set them in the same input capture group.

23.3.8.4 Synchronous Clear Operation by Inter Channel Cooperation

The counters of other channels can be cleared at the same time with the counter clear of some channel caused by the compare match, input capture, saw wave up-count overflow, saw wave down-count underflow, and the GTIOCnA / GTIOCnB pin input selected in the GTCSR register.

The counter clear caused by GTCLR register, external trigger input and the ELC input can perform as synchronous clear when the same counter clear factor is set to target channels of synchronous clear. Therefore, these factors are not prepared for the synchronous clear operation by inter channel cooperation.

Set the channel that generates the synchronization clear source and the channel that is synchronized clear in the same synchronous set/clear group with the GTCR.SSCGRP[1:0] bits.

Similar to the synchronous operation in section 23.3.8.1. Synchronized Operation by Software, if the count clock selected by the GTCR.TPCS [3:0] bits is different for each channel, the synchronous clear operation cannot be performed at exact same timing. Similar to the example of simultaneous clearing operation by software in Figure 23.97, if the count clock is different for each channel, the synchronous clear factor is synchronized with the count clock of each channel before counter clearing.

When either the SSCE bit or the SSCD bit of the GTSECR register is set to 1, the GTCR.SSCEN bits of the channels that selected on the GTSECSR register are set to 0 or 1 and the GTCNT synchronous set/clear function of multiple channels are enabled or disabled at the same time.

Table 23.51 shows synchronous clear factor register setting and Figure 23.100 shows an example of synchronous clear operation by inter channel cooperation and Table 23.52 shows an example for setting synchronous clear operation by inter channel cooperation.

Table 23.51 Synchronous clear factor register setting

Synchronous clear factor by inter channel cooperation	Setting register	Setting value
GTCCRA register compare match/input capture	GTINTAD.SCFA	1b
	GTCSR.CSCMSC[2:0]	001b
GTCCRB register compare match/input capture	GTINTAD.SCFB	1b
	GTCSR.CSCMSC[2:0]	010b
GTCCRC register compare match	GTINTAD.SCFC	1b
	GTCSR.CSCMSC[2:0]	011b
GTCCRD register compare match	GTINTAD.SCFD	1b
	GTCSR.CSCMSC[2:0]	100b
GTCCRE register compare match	GTINTAD.SCFE	1b
	GTCSR.CSCMSC[2:0]	101b
GTCCRF register compare match	GTINTAD.SCFF	1b
	GTCSR.CSCMSC[2:0]	110b
Overflow of Sawtooth-Wave up-count	GTINTAD.SCFPO	1b
Underflow of Sawtooth-Wave down-count	GTINTAD.SCFPU	1b
Clear caused by GTIOCnA/GTIOCnB pin	GTCR.SCGTIOC	1b

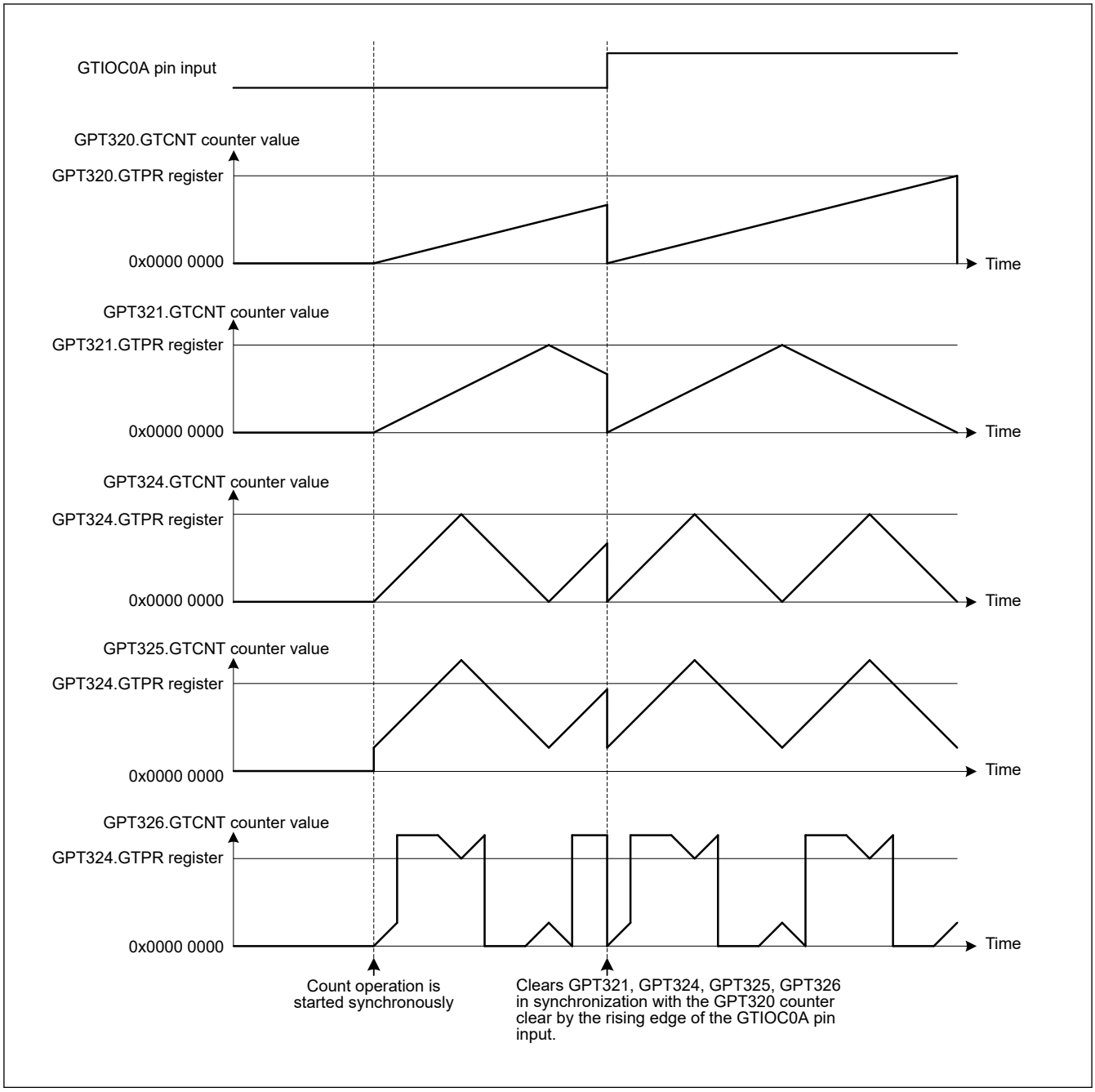


Figure 23.100 Example of Synchronous Clear Operation by Inter Channel Cooperation (GPT320 is saw-wave and counter is cleared by the rising edge of the GTIOC0A, GPT321 is triangle wave, GPT324,5,6 are complementary PWM mode. GPT320,1,4,5,6 are the same synchronous set/clear group)

Table 23.52 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] or GTCR.MD[3:0]. In Figure 23.100, 000b (saw-wave PWM mode 1) is set to GPT320. 100b (triangle-wave PWM mode 1) is set to GPT321. 1100b (complementary PWM mode 1) is set to GPT324(GPT325,6).
2	Set count direction	Select the count direction (up or down) with GTUDDTYC. In Figure 23.100, for GPT320 and GPT321, lower 2 bits of GTUDDTYC is set to 11b, and then lower 2 bits of GTUDDTYC is set to 01b (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of the corresponding channel.

Table 23.52 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation (2 of 2)

No.	Step Name	Description
4	Set cycle	Set the cycle in GTPR of the corresponding channel. When complementary PWM mode, set the cycle in GTPR of the master channel.
5	Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel.
6	Inter channel cooperation synchronous clear setting (Source channel)	Set the GTINTAD register and GTCR.SCGTIOC bit in the source channel of inter channel cooperation synchronous clear to enable synchronous clear. When complementary PWM mode, set GTINTAD of the master channel. In Figure 23.100, GPT320.GTCR.SCGTIOC bit is 1.
7	Inter channel cooperation synchronous clear setting (Cleared channels)	Set GTCSR.CSCMSC[2:0] bits in the cleared channels of inter channel cooperation synchronous clear to select the counter clear by synchronous counter clearing group. When complementary PWM mode, set GTCSR of the master channel. In Figure 23.100, GTCSR.CSCMSC[2:0] bits of GPT321, GPT324, GPT325 and GPT326 is 111b.
8	Set group of inter channel cooperation synchronous clear	Set the same value to GTCR.SSCGRP[1:0] bits in the source channel and cleared channels of inter channel cooperation synchronous clear and set them in the same synchronous set/clear group. When complementary PWM mode, set GTCR of the master channel.
9	Enable inter channel cooperation synchronous clear	Set GTCR.SSCEN bits in the source channel and cleared channels of inter channel cooperation synchronous clear to enable synchronous clear.

Table 23.53 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation (Clear caused by the GTCCRA input capture using the GTIOCnA/GTIOCnB pin)

Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or the GTCR.MD[3:0] bits.
Set count direction	Select the count direction (up or down) with the GTUDDTYC register.
Select count clock	Select the count clock with GTCR.TPCS[2:0] bits of the corresponding channel, or Select the count clock with GTCR.TPCS [3:0] bits of the corresponding channel
Period setting	Set a period in the GTPR register of the corresponding channel. When complementary PWM mode, set a period in the GTPR register of the master channel.
Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel.
Inter channel cooperation synchronous clear setting (Source channel)	Set the input capture factor using the GTIOCnA/B pin to the GTICASR register and set the same factor as the GTICASR register to the GTCSR register as the count clearing factor. In addition, Set GTINTAD.SCFA bit=1b and GTCSR.CSCMSC[2:0] bit=001b to enable synchronous clear source by the GTCCRA input capture. When complementary PWM mode, set the GTINTAD register of the master channel.
Inter channel cooperation synchronous clear setting (Cleared channels)	Set the same value to the GTCR.SSCGRP[1:0] bits in the source channel and cleared channels of inter channel cooperation synchronous clear and set them in the same synchronous set/clear group. When complementary PWM mode, set the GTCR register of the master channel.
Enable inter channel cooperation synchronous clear	Set the GTCR.SSCEN bits in the source channel and cleared channels of inter channel cooperation synchronous clear to enable synchronous clear.

23.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 14 × 2 phases of linked PWM waveforms for a maximum of GPT × 14 channels.

Figure 23.101 shows an example in which four channels perform synchronized operation in saw-wave PWM mode 1 and eight phases of PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

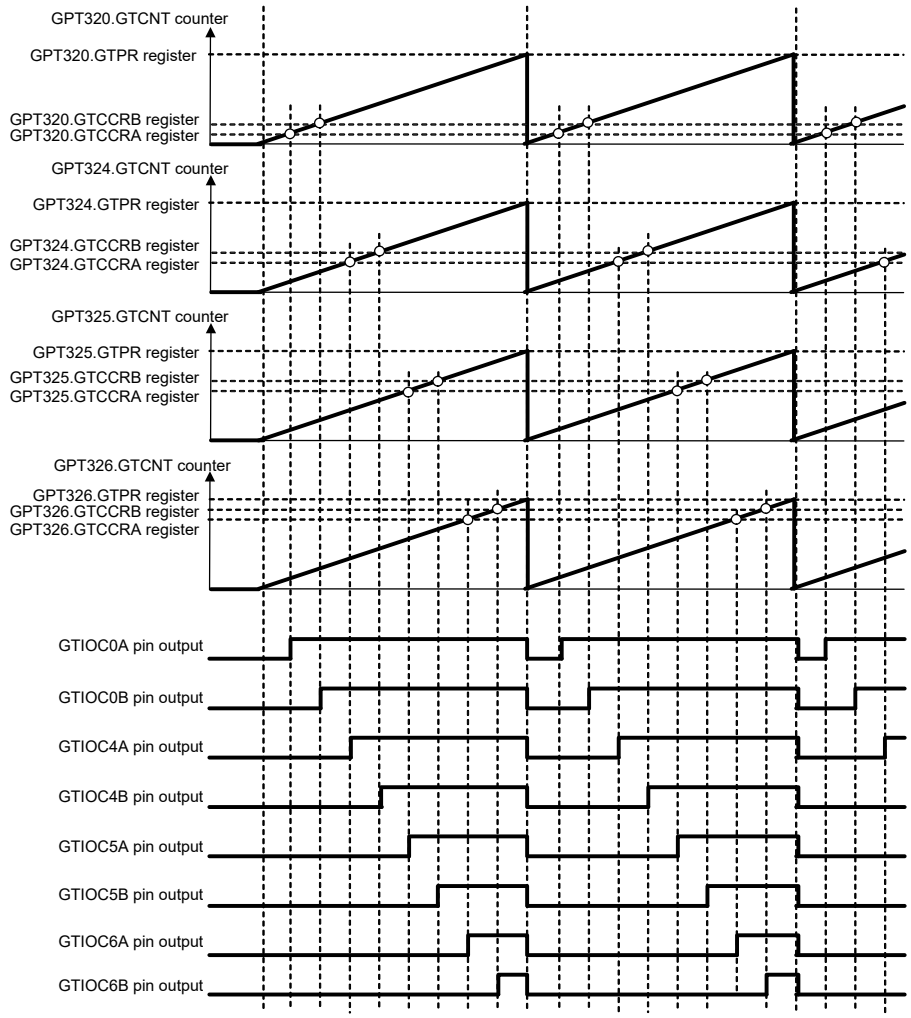


Figure 23.101 Example of synchronized PWM output

(2) 3-phase saw-wave complementary PWM output

Figure 23.102 shows an example in which three channels perform synchronized operation in saw-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

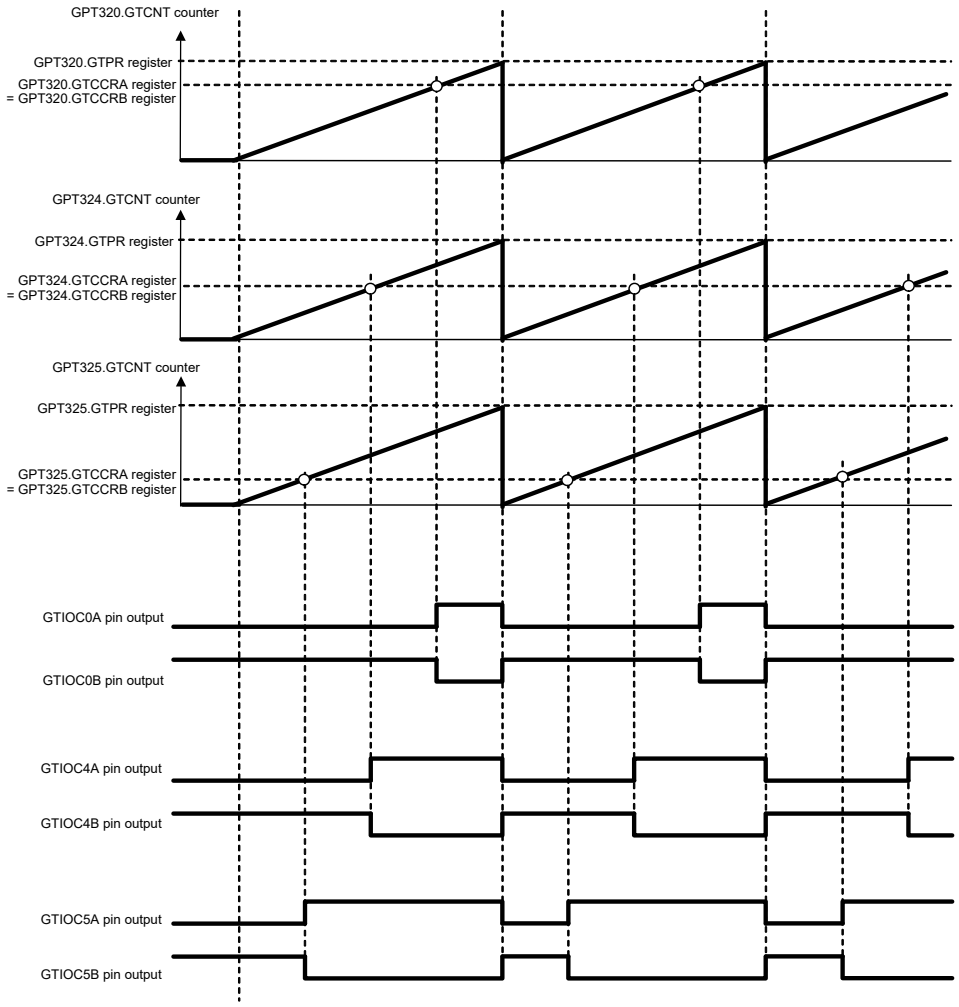


Figure 23.102 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 23.103 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTIOCnB compare match, and retains the output at the cycle end.

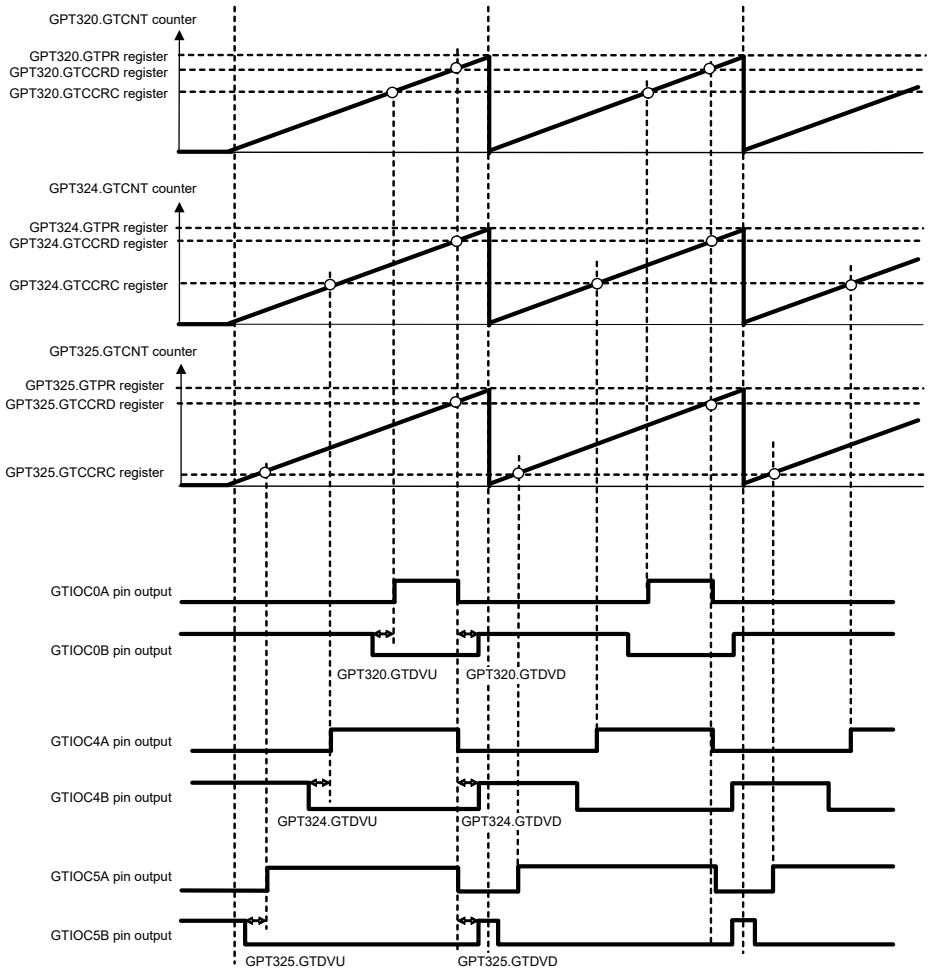


Figure 23.103 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 23.104 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

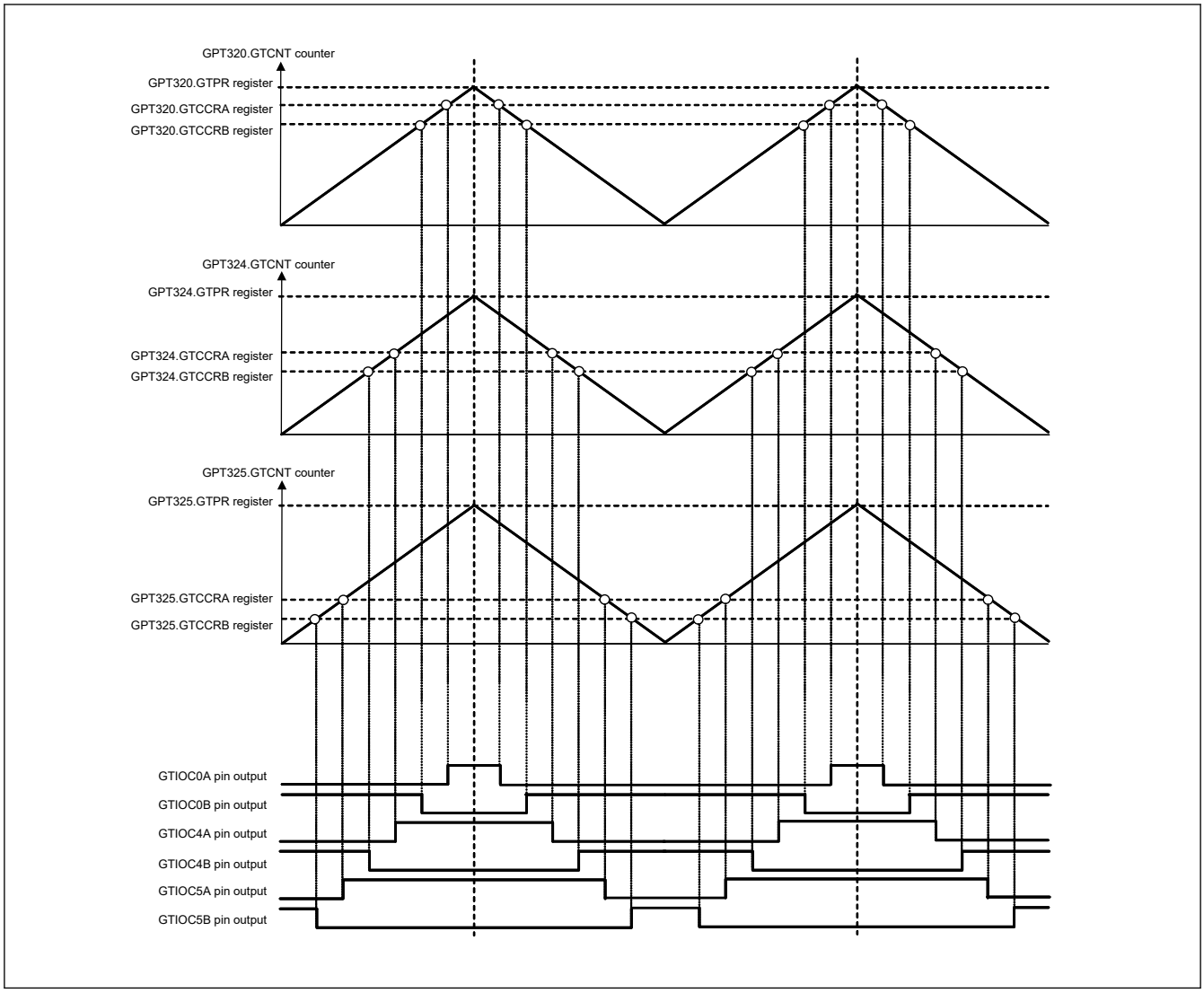


Figure 23.104 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 23.105 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

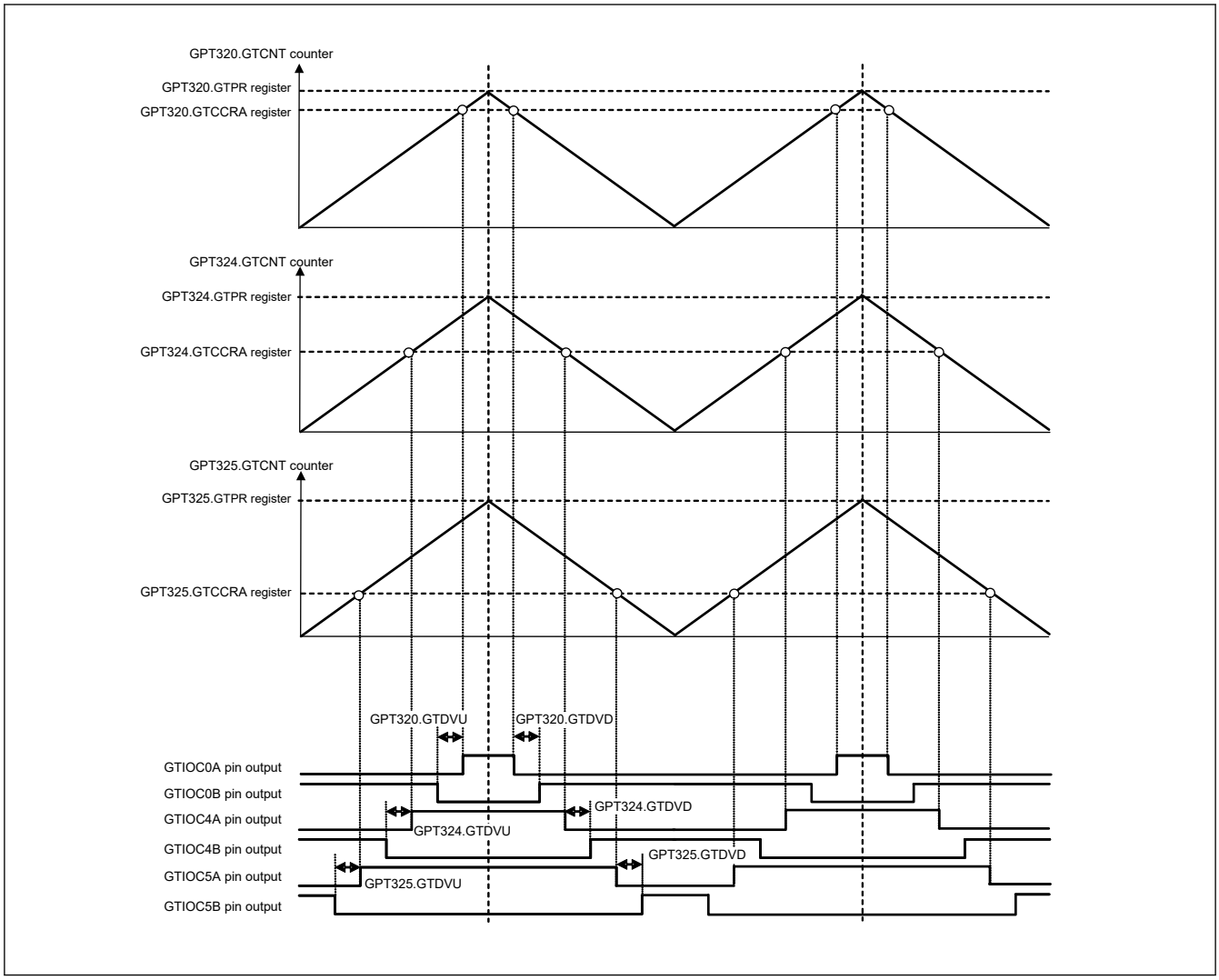


Figure 23.105 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 23.106 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

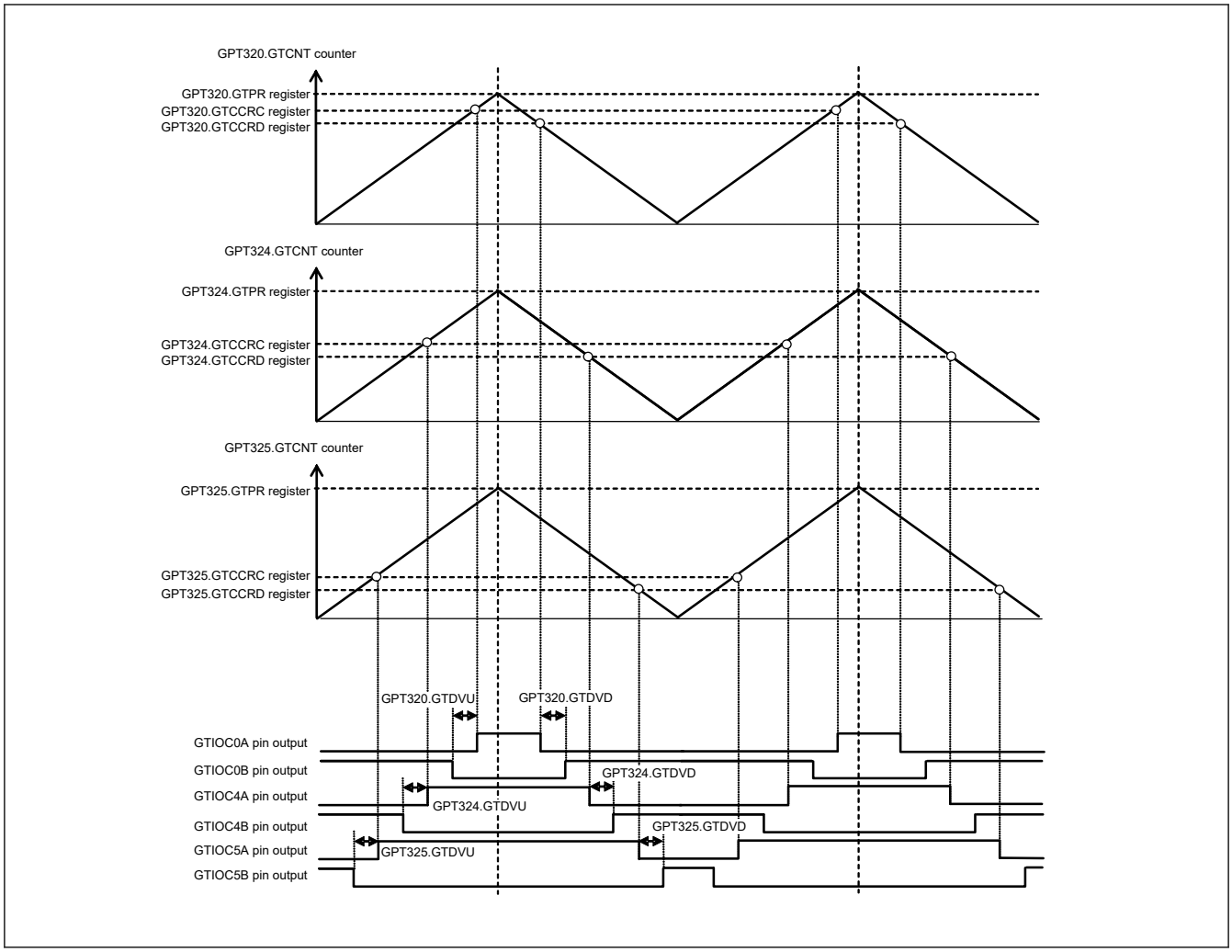


Figure 23.106 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

23.3.10 Period Count Function

By setting the GTPC register, the end of period can be counted.

The number of period to be counted should be set into the GTPC.PCNT counter when the GTPC.PCEN bit is 0. When the PCEN bit is 1, the PCNT counter can be read, but writing is disabled. When the PCEN bit is 1, down-counting is performed at the end of period. When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped to finish the period count function. At that time, the GTST.PCF flag is set, and the period count function finish interrupt request GPTn_PC is generated. When the GTPC.ASTP bit is 1, the GTCNT counter is also stopped at the same time that the period count function is finished.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immediately after that.

When either GTSECR.SPCE bit or GTSECR.SPCD bit is set to 1, the PCEN bit in the channels set to 1 by the GTSECSR register is simultaneously set the value to enable or disable the period count function for multiple channels.

Figure 23.107 and Figure 23.108 show examples of PWM cycle count function.

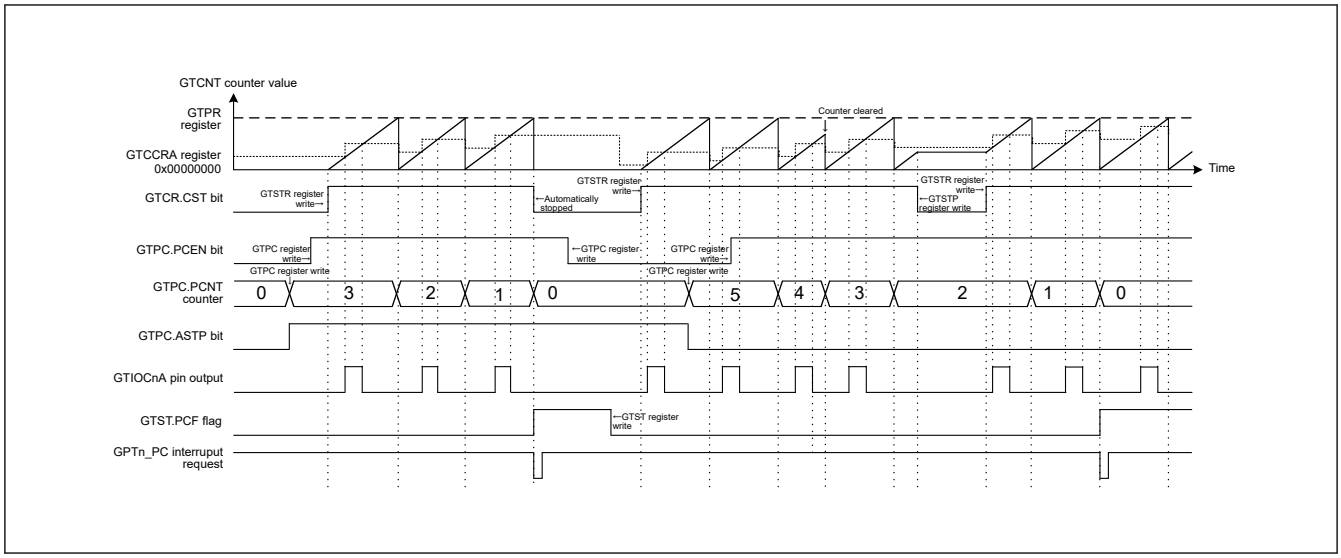
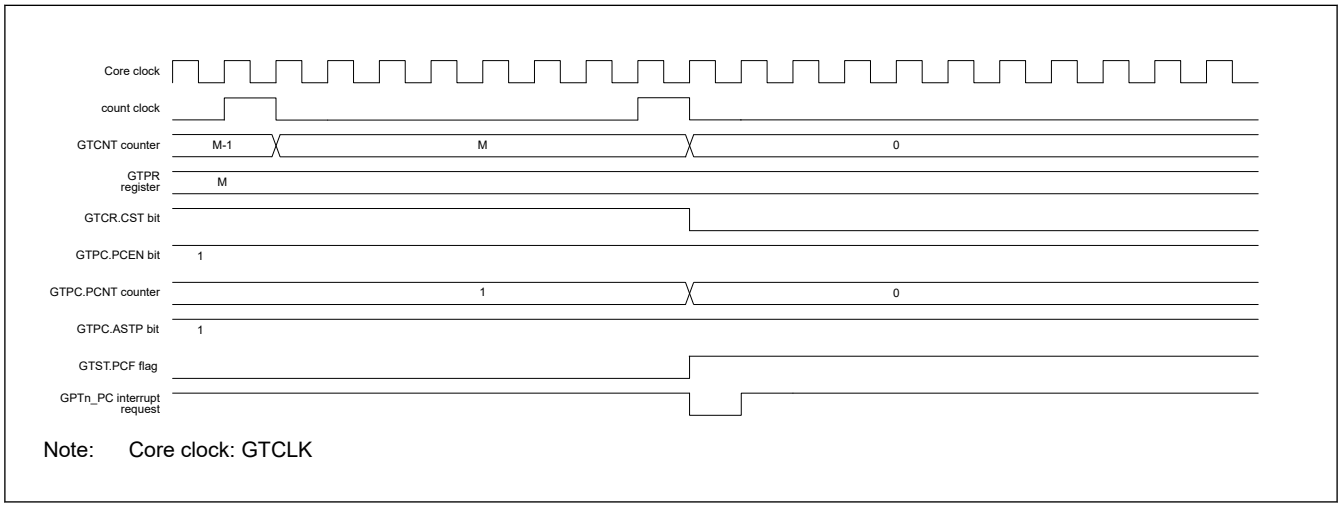


Figure 23.107 Example of PWM cycle count function (saw-wave one-shot pulse mode)



Note: Core clock: GTCLK

Figure 23.108 Example of the timing of operations for PWM cycle count function (saw-wave one-shot pulse mode, up-counting)

23.3.11 Phase Counting Function

The phase difference between the GTIOCnA and GTIOCnB pin (n = 0 to 13) inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCnA and GTIOCnB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 23.3.1.1. Counter Operation.

Figure 23.109 to Figure 23.118 show an example of phase counting modes 1 to 5 operation when the GTIOCnA, GTIOCnB pins are used. Table 23.54 to Table 23.63 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers which is corresponding to Figure 23.109 to Figure 23.118.

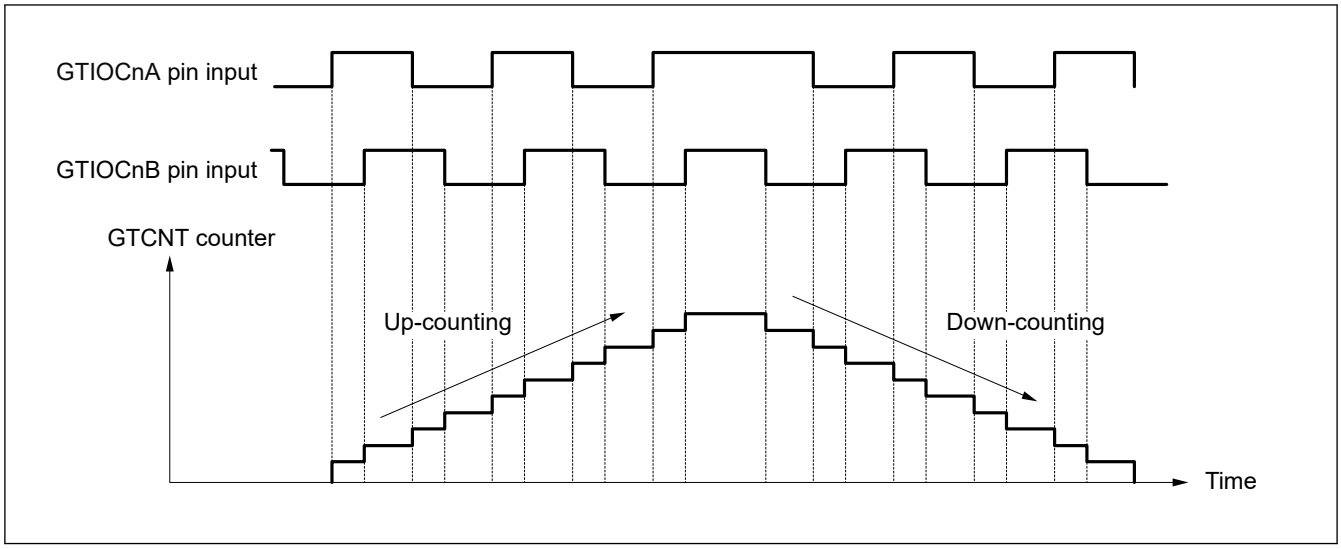


Figure 23.109 Example of phase counting mode 1

Table 23.54 Conditions of up-counting/down-counting in phase counting mode 1

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

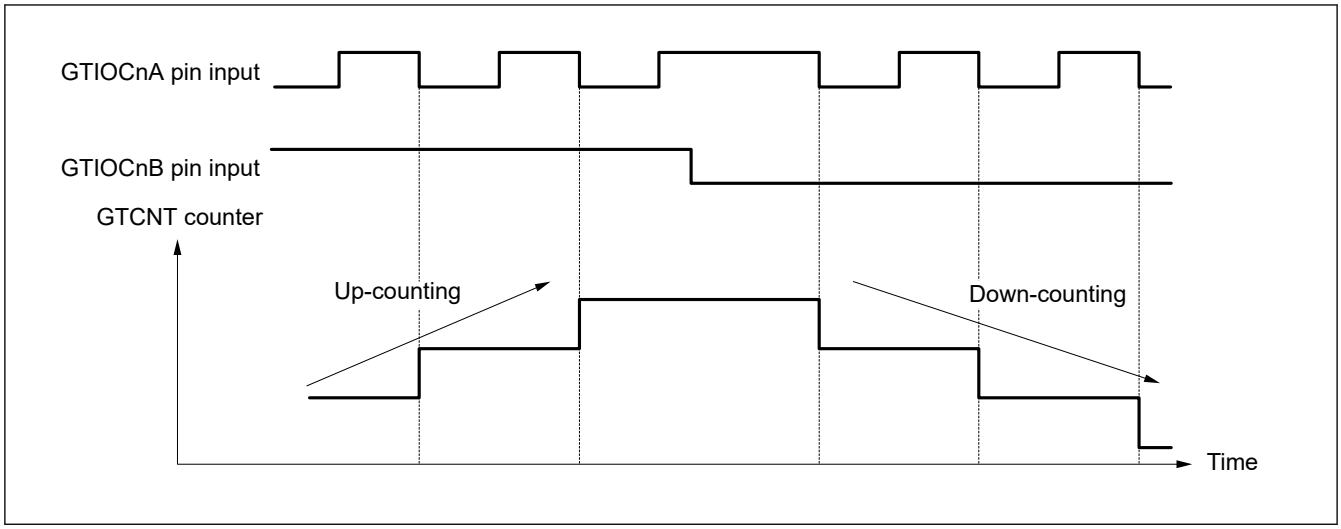


Figure 23.110 Example of phase counting mode 2 (A)

Table 23.55 Conditions of up-counting/down-counting in phase counting mode 2 (A)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Down-counting	

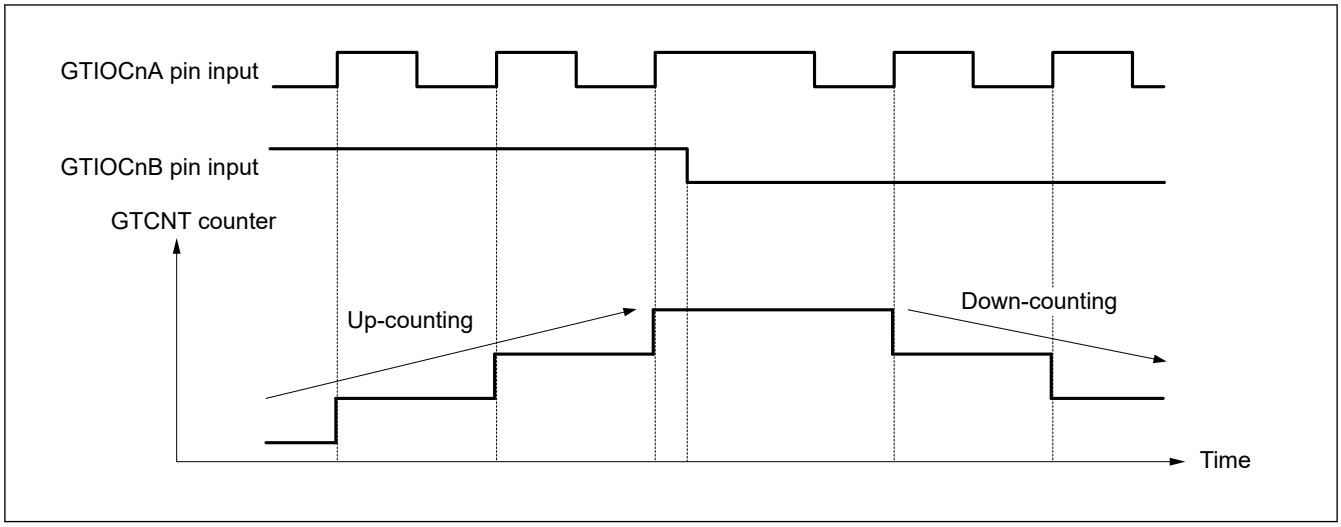


Figure 23.111 Example of phase counting mode 2 (B)

Table 23.56 Conditions of up-counting/down-counting in phase counting mode 2 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	Not counting	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

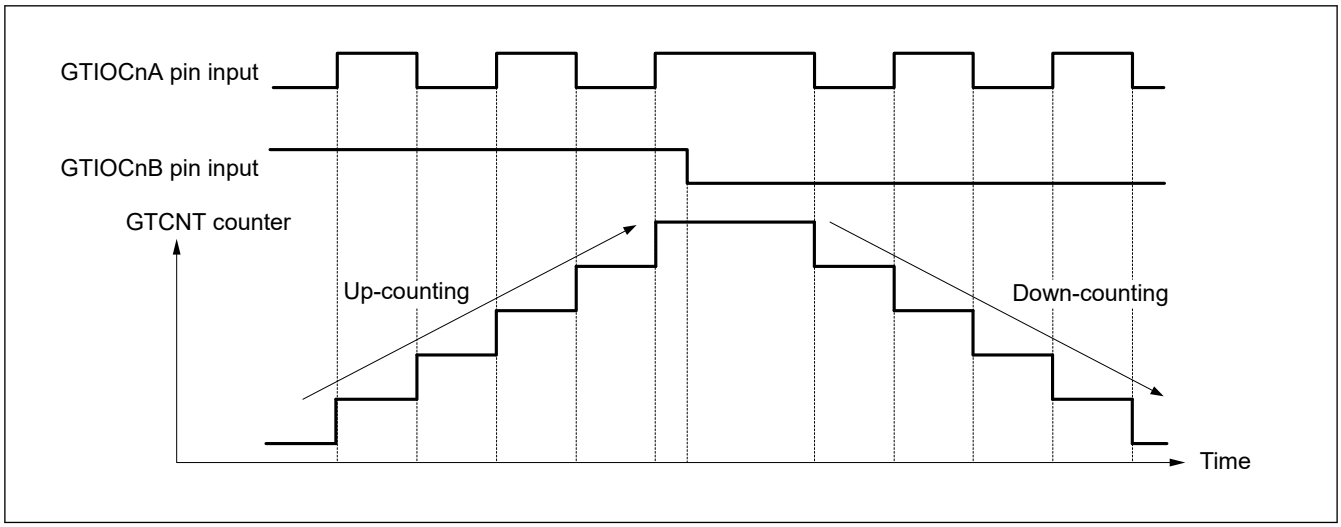


Figure 23.112 Example of phase counting mode 2 (C)

Table 23.57 Conditions of up-counting/down-counting in phase counting mode 2 (C)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

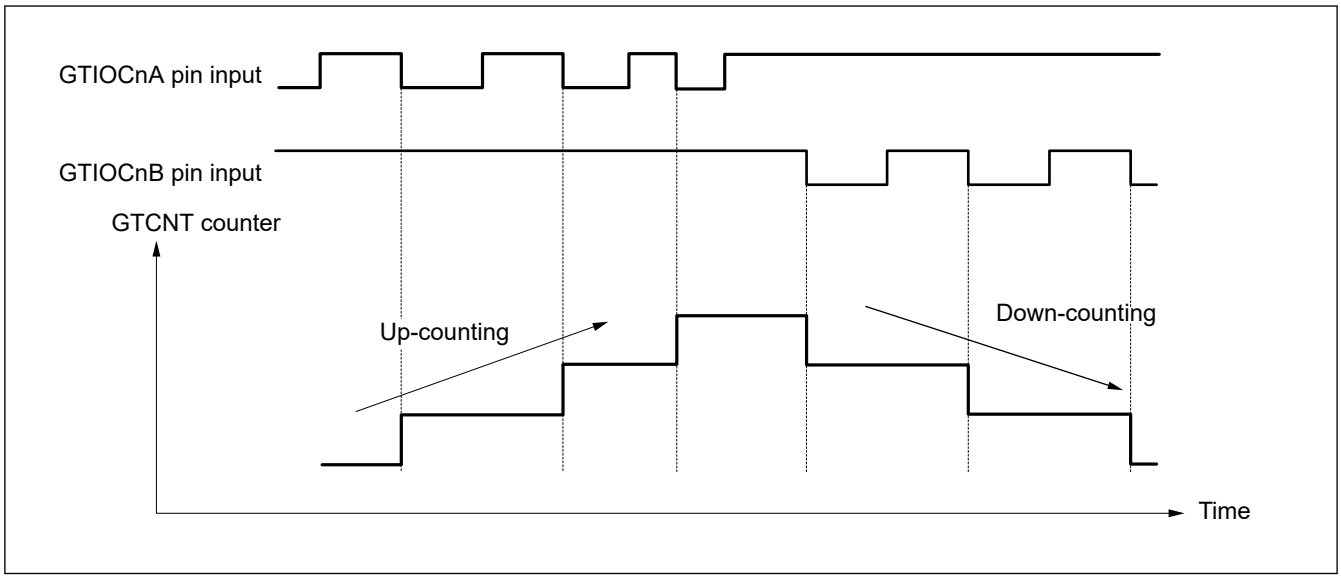


Figure 23.113 Example of phase counting mode 3 (A)

Table 23.58 Conditions of up-counting/down-counting in phase counting mode 3 (A)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

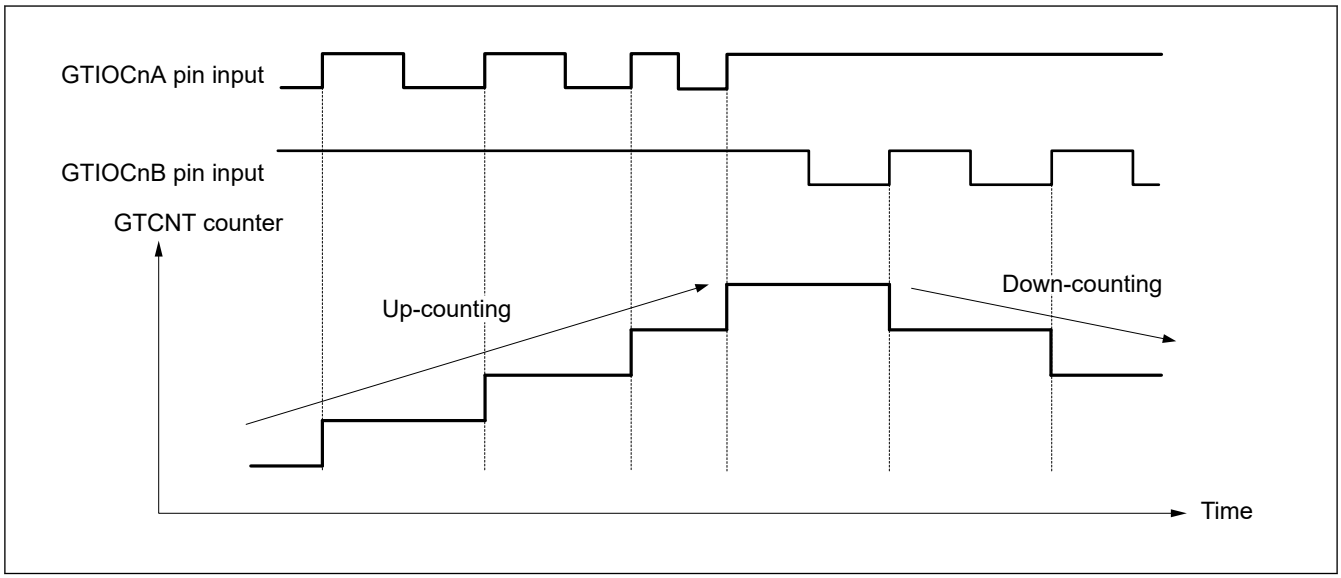


Figure 23.114 Example of phase counting mode 3 (B)

Table 23.59 Conditions of up-counting/down-counting in phase counting mode 3 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	Not counting	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

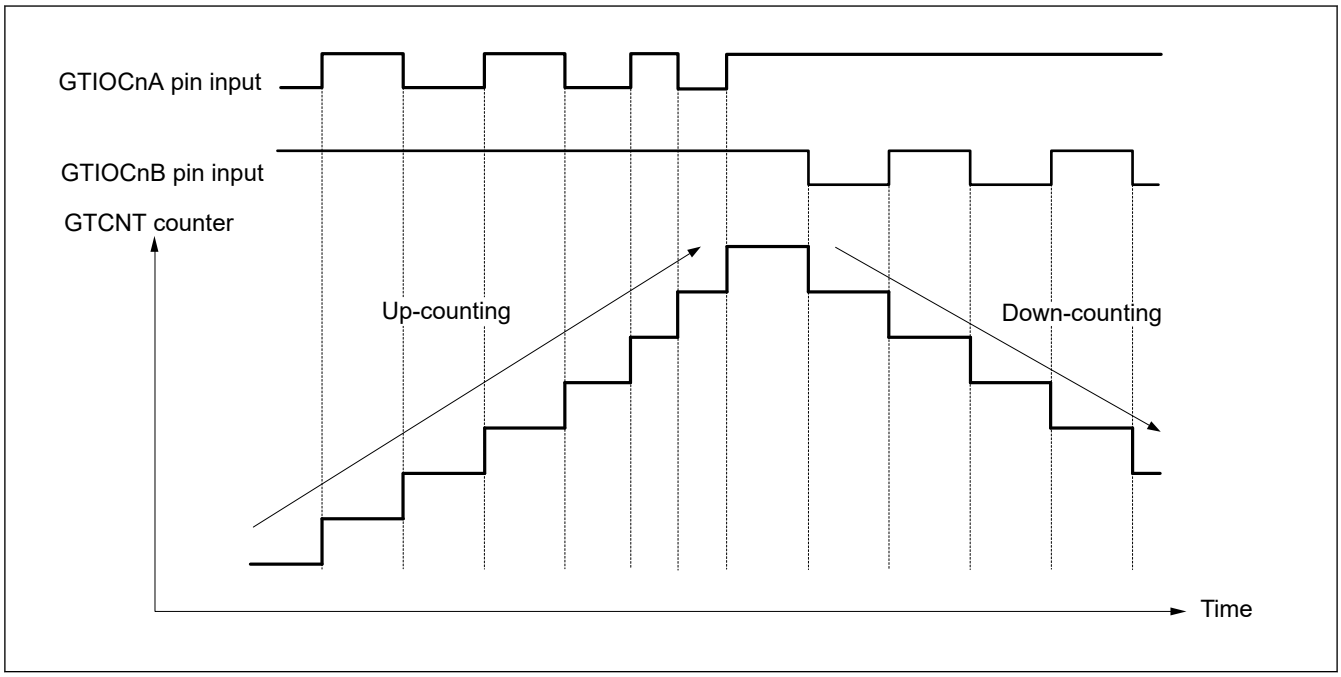


Figure 23.115 Example of phase counting mode 3 (C)

Table 23.60 Conditions of up-counting/down-counting in phase counting mode 3 (C)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	Not counting	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High	Up-counting	
↓	Low	Not counting	

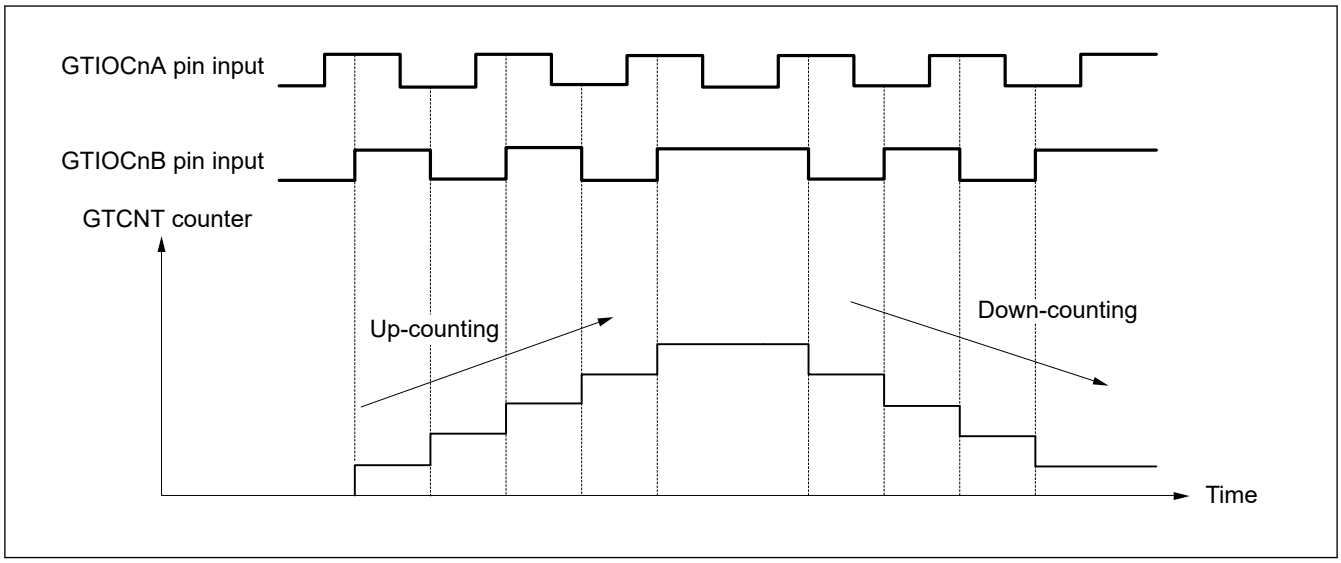


Figure 23.116 Example of phase counting mode 4

Table 23.61 Conditions of up-counting/down-counting in phase counting mode 4

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	Not counting	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Not counting	
↓	Low		

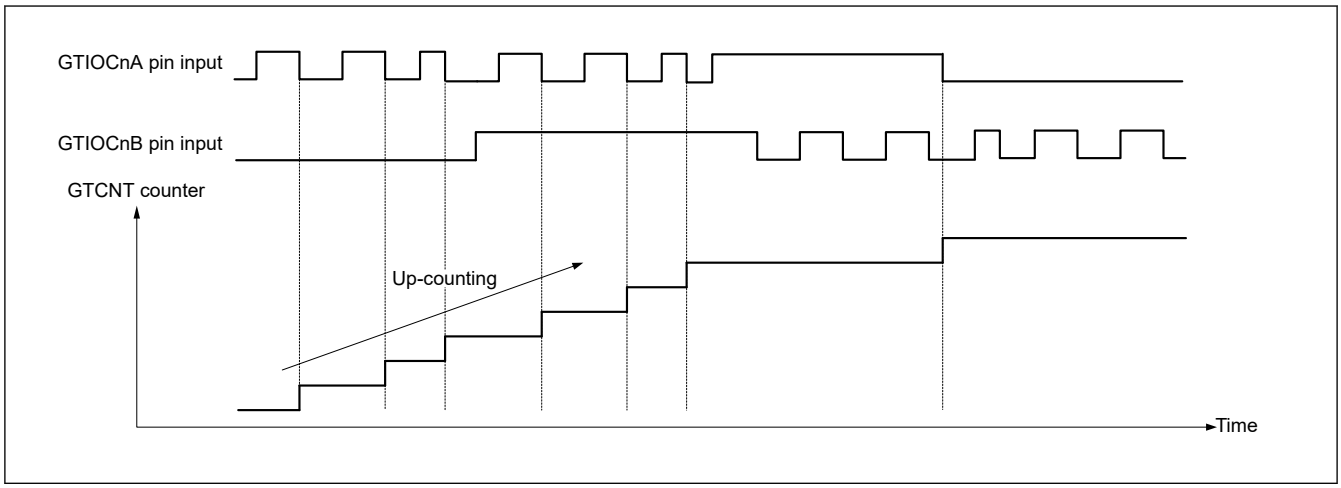


Figure 23.117 Example of phase counting mode 5 (A)

Table 23.62 Conditions of up-counting/down-counting in phase counting mode 5 (A)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Up-counting	

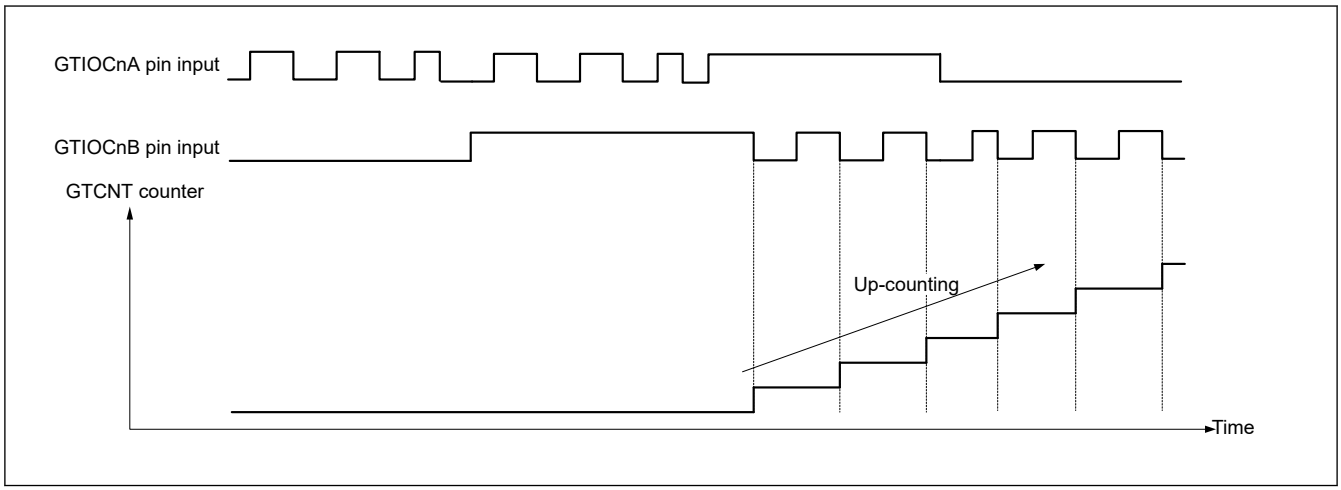


Figure 23.118 Example of phase counting mode 5 (B)

Table 23.63 Conditions of up-counting/down-counting in phase counting mode 5 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low	↓	Up-counting	
↑	Low	Not counting	
↓	High		
High	↓	Up-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

23.3.12 External Pulse Width Measuring Function

The pulse width of GTIOCnA pin input (n = 0 to 3), GTIOCnB pin input, and GTETRGA / GTETRGB / GTETRGC / GTETRGD pin inputs can be measured.

The setting to enable or disable count-up of the GTCNT counter and the input pin and level which measured pulse width are selected by the USILVL[3:0] bits of the GTUPSR register.

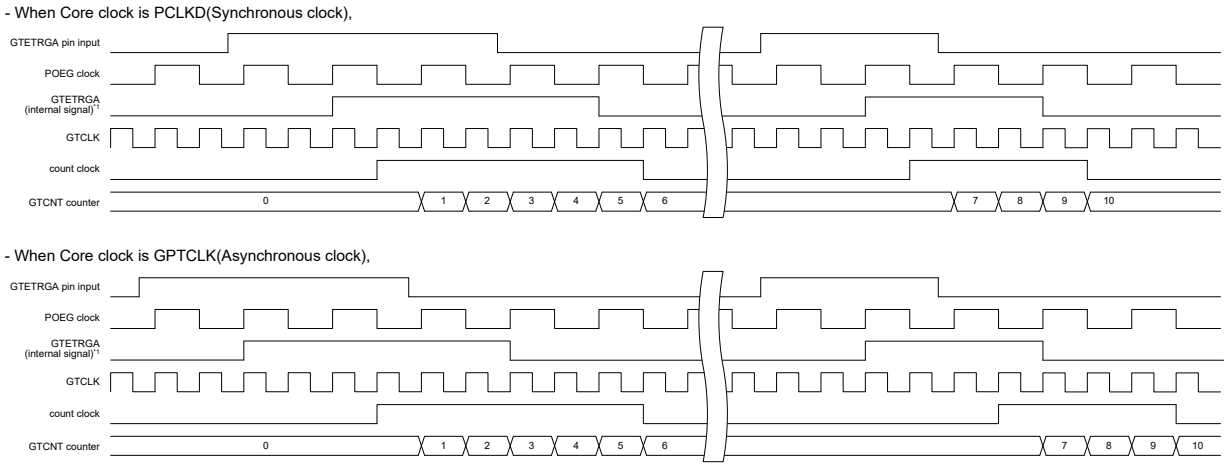
The setting to enable or disable count-down of the GTCNT counter and the input pin and level which measured pulse width are selected by the DSILVL[3:0] bits of the GTDNSR register.

The setting to enable both count-up and count-down of the GTCNT counter at the same time is prohibited.

The counting operation performs periodic counting with the period of the GTPR register.

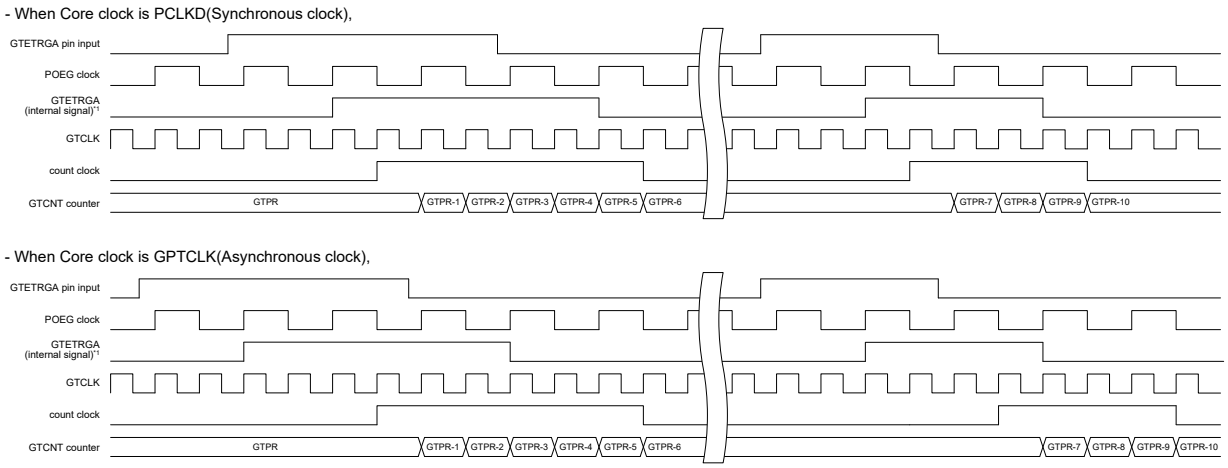
If the phase counting function and the pulse width measuring function are enabled at the same time, the pulse width measuring function does not work and the phase counting function works.

Figure 23.119, Figure 23.120 show examples of external pulse width measuring function and Table 23.64 shows example for setting external pulse width measuring function.



Note: POEG clock: PCLKB
Note 1. The input signal to GPT when the digital noise filter of GTETRGA pin is not used in POEG is shown.

Figure 23.119 Example of External pulse width measuring function(Up-counting)



Note: POEG clock: PCLKB
Note 1. The input signal to GPT when the digital noise filter of GTETRGA pin is not used in POEG is shown.

Figure 23.120 Example of External pulse width measuring function(Down-counting)

Table 23.64 Example for Setting External pulse width measuring function

No.	Step Name	Description
1	Set external pulse width measuring function	Enable external pulse width measuring function with the GTUPSR.USILVL[3:0] bits for up-counting operation and the GTDNSR.DSILVL[3:0] bits for down-counting operation and select the input pin and level to measure. In Figure 23.119, GTUPSR.USILVL[3:0] = 1001b (count up when GTETRGA pin is 1), In Figure 23.120, GTDNSR.DSILVL[3:0] = 1001b (count down when GTETRGA pin is 1)
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of the corresponding channel.
3	Set cycle	Set the cycle in GTPR of the corresponding channel.
4	Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel. In Figure 23.119, 0000 0000h is set. In Figure 23.120, the GTPR register value is set.
5	Start count operation	Input a pulse to the input pin to be measured to start count operation.

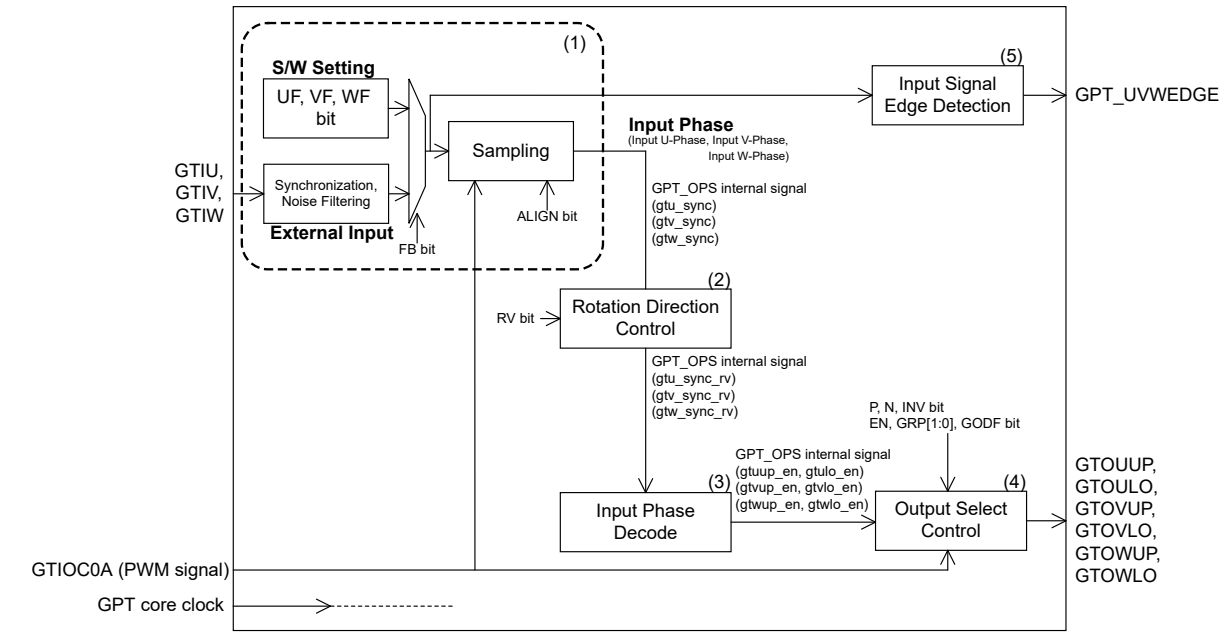
23.3.13 Output Phase Switching (GPT_OPS)

GPT_OPS can easily control Brushless DC motor using Output Phase Switching Control Register (OPSCR).

GPT_OPS uses S/W setting value (OPSCR.UF, VF, WF bits) or external signals detected by the Hall element as input signals. GPT_OPS outputs either level signals or chopped signals by GPT320's PWM as the 6-phase (U-positive phase / negative phase, V-positive phase / negative phase, W-positive phase / negative phase) signals to control motor.

Figure 23.121 shows the block diagram of GPT_OPS.

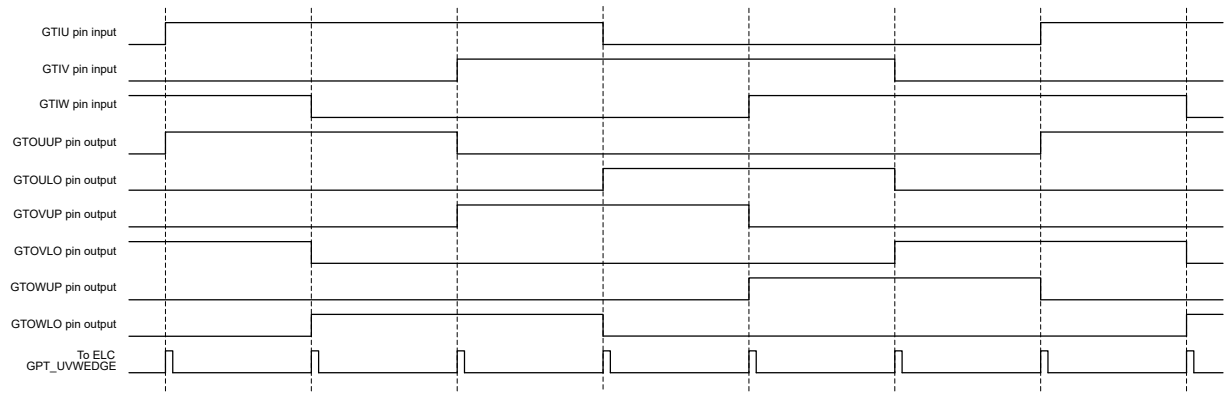
The GPT_UVWEDGE signal is output signal to ELC generated by detecting the edge of input signal.



Note: GPT core clock: GTCLK (PCLKD or GPTCLK)

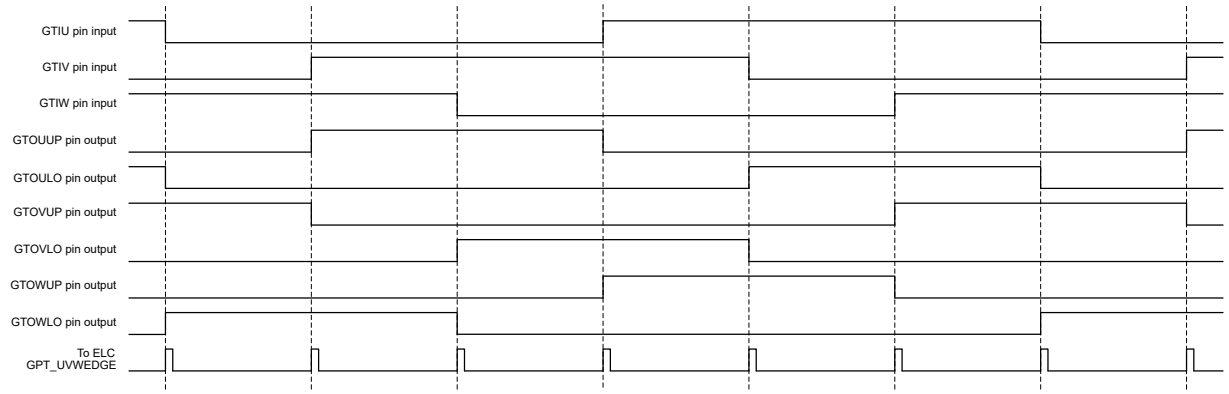
Figure 23.121 GPT_OPS Block Diagram

Figure 23.122 and Figure 23.123 show examples of GPT_OPS level output operation.



Note: Register settings: OPSCR.FB = 0, OPSCR.RV = 0, OPSCR.P = 0, OPSCR.N = 0, OPSCR.INV = 0

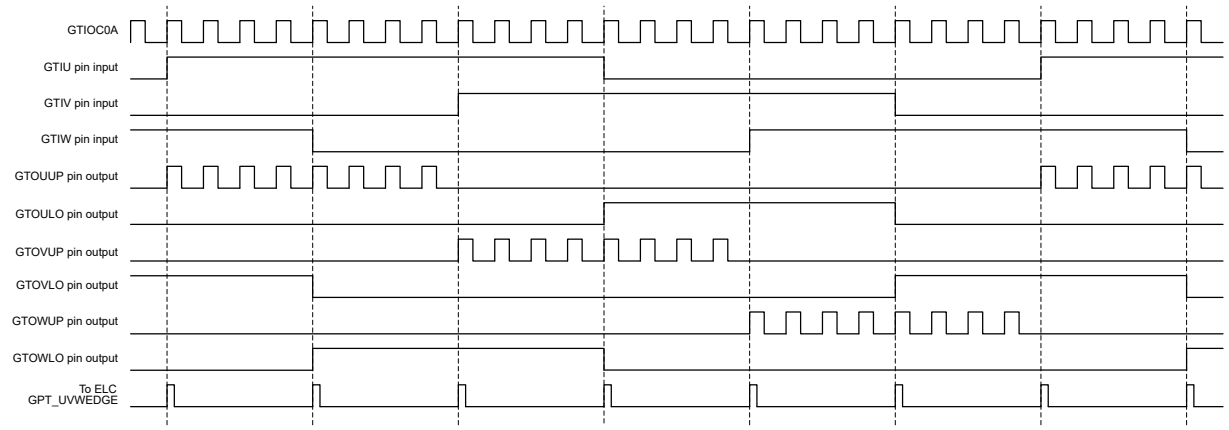
Figure 23.122 Example of GPT_OPS Level Output Operation (Forward Rotation)



Note: Register settings: OPSCR.FB = 0, OPSCR.RV = 1, OPSCR.P = 0, OPSCR.N = 0, OPSCR.INV = 0

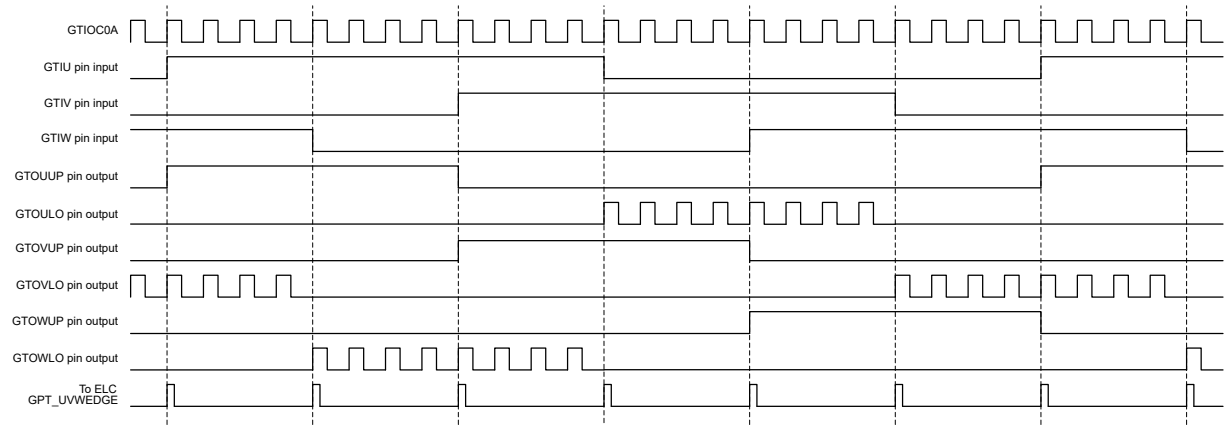
Figure 23.123 Example of GPT_OPS Level Output Operation (Reverse Rotation)

Figure 23.124 and Figure 23.125 show examples of GPT_OPS chopped output operation.



Note: Register settings: OPSCR.FB = 0, OPSCR.RV = 0, OPSCR.P = 1, OPSCR.N = 0, OPSCR.INV = 0

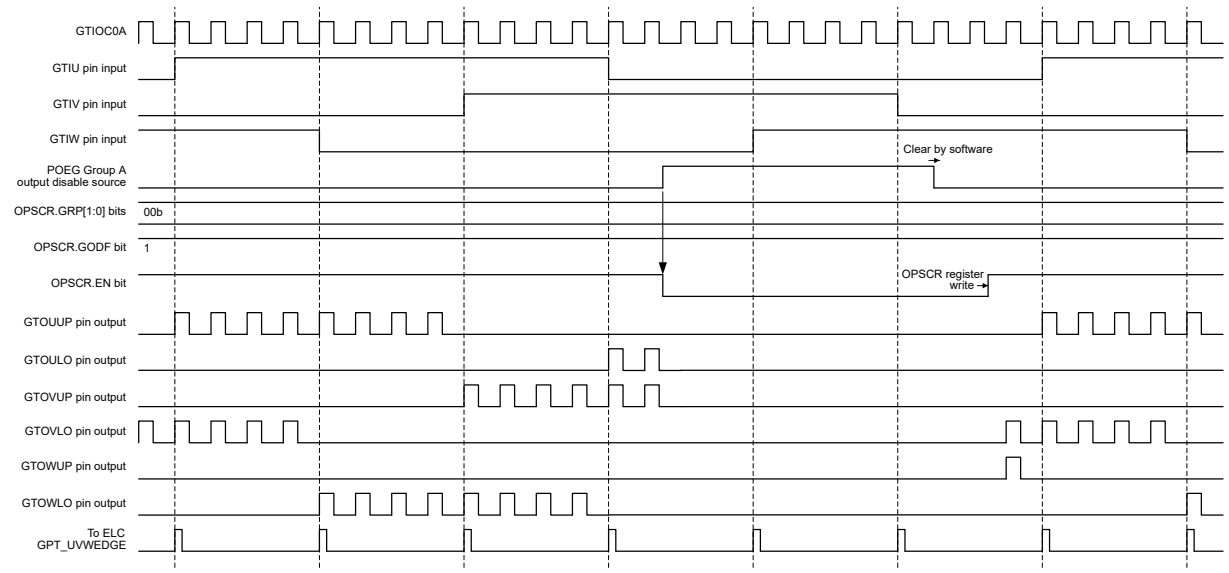
Figure 23.124 Example of GPT_OPS Chopped Output Operation (Positive Phase 120-degree)



Note: Register settings: OPSCR.FB = 0, OPSCR.RV = 0, OPSCR.P = 0, OPSCR.N = 1, OPSCR.INV = 0

Figure 23.125 Example of GPT_OPS Chopped Output Operation (Negative Phase 120-degree)

Figure 23.126 shows an example of GPT_OPS output disable control operation.



Note: Register settings: OPSCR.FB = 0, OPSCR.RV = 0, OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0

Figure 23.126 Example of GPT_OPS Output Disable Control Operation

23.3.13.1 Input Selection and Sampling

The FB bit selects either the software setting value or external input for the input signal.

When the FB bit is 0, the GTIU, GTIV, GTIW external input are selected for the input signal to GPT_OPS after synchronization with the GPT core clock (GTCLK) and noise filtering.

When the FB bit is 1, the software setting value (UF, VF, WF bits) are selected for the input signal to GPT_OPS.

The selected input signals are sampled by the method selected by the ALIGN bit, and they are treated as input phase of GPT_OPS.

When the ALIGN bit is 0, the input signals are sampled by GTCLK.

When the ALIGN bit is 1, the input signals are sampled by the falling edge of GTIOC0A pin output.

The signals after sampling can be read by the U, V, W bits.

Table 23.65 shows the input selection by the FB bit and sampling method by the ALIGN bit.

Table 23.65 Input Selection and Sampling Method

OPSCR Register		Input Selection Sampling Method	Input Phase (GPT_OPS internal signal)
FB bit	ALIGN bit		
0	0	GTIU, GTIV, GTIW external input GTCLK sampling	Input U-phase (gtu_sync) Input V-phase (gtv_sync) Input W-phase (gtw_sync)
	1	GTIU, GTIV, GTIW external input GTIOC0A falling edge sampling	
1	0	Software setting value UF, VF, WF bits GTCLK sampling	
	1	Software setting value UF, VF, WF bits GTIOC0A falling edge sampling	

23.3.13.2 Rotation Direction Control

When the rotation direction is reverse (RV bit = 1), the input phase is inverted.

23.3.13.3 Input Phase Decode

The 6-phase signals by decoding input phase after rotation direction control are generated.

Table 23.66 and Table 23.67 show the decode tables of input phase to rotate motor in forward (RV = 0) and reverse (RV = 1).

Table 23.66 The Decode Table of Input Phase (Forward Rotation)

	Input Phase			Input Phase after Rotation Direction Control			6-Phase Signals					
	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase	U Positive Phase	U Negative Phase	V Positive Phase	V Negative Phase	W Positive Phase	W Negative Phase
	gtu_sync	gtv_sync	gtw_sync	gtu_sync_rv	gtv_sync_rv	gtw_sync_rv	gtuup_en	gtulo_en	gtvup_en	gtvlo_en	gtwup_en	gtwlo_en
	1	0	1	1	0	1	1	0	0	1	0	0
	1	0	0	1	0	0	1	0	0	0	0	1
	1	1	0	1	1	0	0	0	1	0	0	1
	0	1	0	0	1	0	0	1	1	0	0	0
	0	1	1	0	1	1	0	1	0	0	1	0
	0	0	1	0	0	1	0	0	0	1	1	0
	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	0	0	0	0	0	0

Table 23.67 The Decode Table of Input Phase (Reverse Rotation)

	Input Phase			Input Phase after Rotation Direction Control			6-Phase Signals					
	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase	U Positive Phase	U Negative Phase	V Positive Phase	V Negative Phase	W Positive Phase	W Negative Phase
	gtu_sync	gtv_sync	gtw_sync	gtu_sync_rv	gtv_sync_rv	gtw_sync_rv	gtuup_en	gtulo_en	gtvup_en	gtvlo_en	gtwup_en	gtwlo_en
	1	0	1	0	1	0	0	1	1	0	0	0
	1	0	0	0	1	1	0	1	0	0	1	0
	1	1	0	0	0	1	0	0	0	1	1	0
	0	1	0	1	0	1	1	0	0	1	0	0
	0	1	1	1	0	0	1	0	0	0	0	1
	0	0	1	1	1	0	0	0	1	0	0	1
	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	0	0	0	0	0	0

23.3.13.4 Output Selection Control

The EN, P, N, INV bits select the output wave.

The EN bit enables output of the 6-phase output. When the EN bit is 1, output of the 6-phase output is enabled. When the EN bit is 0, the external pin output is Hi-Z.

The P, N bits select whether chopping positive and negative phase are performed or not. When P, N bits are 1, chopping is performed by GTIOC0A pin output.

When the chopping is performed, there are cases where the PWM width of output is shorter than the width of the PWM used to chop just before or after switching of output phase, depending on the phase difference between the phase output switch timing and the phase of PWM.

The INV bit selects the polarity (either positive logic or negative logic) of phase output.

Table 23.68 and Table 23.69, show the output selection control method for positive and negative phase output.

Table 23.68 Output Selection Control Method (Positive Phase)

EN bit	P bit	INV bit	GTOUUP / GTOVUP / GTOWUP
0	x	x	0 (External pin output is Hi-Z)
1	0	0	Positive logic level output (gtuup_en) (gtvup_en) (gtwup_en)
1	0	1	Negative logic level output (~gtuup_en) (~gtvup_en) (~gtwup_en)
1	1	0	Positive logic chopped output (GTIOC0A & gtuup_en) (GTIOC0A & gtvup_en) (GTIOC0A & gtwup_en)
1	1	1	Negative logic chopped output (~(GTIOC0A & gtuup_en)) (~(GTIOC0A & gtvup_en)) (~(GTIOC0A & gtwup_en))

Table 23.69 Output Selection Control Method (Negative Phase)

EN bit	N bit	INV bit	GTOULO / GTOVLO / GTOWLO
0	x	x	0 (External pin output is Hi-Z)
1	0	0	Positive logic level output (gtulo_en) (gtvlo_en) (gtwlo_en)
1	0	1	Negative logic level output (~gtulo_en) (~gtvlo_en) (~gtwlo_en)
1	1	0	Positive logic chopped output (GTIOC0A & gtulo_en) (GTIOC0A & gtvlo_en) (GTIOC0A & gtwlo_en)
1	1	1	Negative logic chopped output (~(GTIOC0A & gtulo_en)) (~(GTIOC0A & gtvlo_en)) (~(GTIOC0A & gtwlo_en))

23.3.13.5 Output Selection Control (Group Output Disable Function)

When GODF = 1 and signal value selected by the GRP bit is Hi (Output Disable Request), GPT_OPS's output pins are changed to Hi-Z asynchronously and the OPSCR.EN bit is cleared to 0 by the output disable request signal synchronized with GTCLK.

For the return, after clearing the Output Disable Request by software, set the EN bit to 1.

The timing of EN bit cleared to 0 is 3 GTCLK cycles after generating the output disable request. In order to perform the output disable control surely, the output disable request flag in POEG should be cleared in the timing that terminating the output disable request is at least 4 GTCLK cycles after generating the output disable request.

The example of the operation of the group output disable control, see the above-mentioned Figure 23.126.

23.3.13.6 Event Link Controller (ELC) Output

The logical sum of the pulse detected by rising and falling edge of U, V, W phase input is output to the event link controller (ELC). When the high level period of input phase is short, there are cases that the detected edge is not transmitted to the ELC correctly because of the logical sum.

23.3.13.7 GPT_OPS Start Operation Setting Flow

Table 23.70 Example for Setting of GPT_OPS Start Operation

No.	Step Name	Description
1	Set Operation Mode of GPT320	Set the PWM output operation mode of GPT320. See section 23.3.3. PWM Output Operating Mode
2	Start Count Operation of GTP320	Start count operation of GPT320, and outputs PWM waveform.
3	Set GPT_OPS Input Condition	● When the soft setting is selected, set the soft setting values in the UF, VF, WF bits. ● When the external input is selected, if necessary, use noise filtering. Select the sampling clock for external input into NFCS[1:0] bits, and set NFEN bit to 1.
4	Select GPT_OPS Input phase and Alignment	Select input phase by FB bit. Select alignment of input phase by ALIGN bit.
5	Set GPT_OPS Output phase Condition	Set the rotation direction by RV bit. Select whether chopping is performed or not by P, N bits. Select the output polarity by INV bit.
6	Set GPT_OPS Output Disable Condition	Select the error group by GRP[1:0] bits Set ON/OFF of the group output disable function by GODF bit.
7	Set GPT_OPS Operation	Set EN bit to 1 to output the 6-phase output to drive the brushless DC motor.

23.3.14 Inter Channel Logical Operation Function

The logical operation function between compare match outputs can be performed.

Figure 23.127 shows the block diagram of inter channel logical operation.

To prevent hazard to the GPT output, the signal after logical operation is latched with GTCLK. After latching, the output disable control is performed.

When the logical operation function which causes the delay of 1 GTCLK is selected, the output enable signal is also delayed with 1 GTCLK and input to the output disable control.

When the same signal (C = A or D = B) to operate logical function AND, OR, EXOR and NOR is selected, C or D is treated as 1. In the case of GTIOCnA pin output, when A of same channel is selected for C, the result of AND is A, the result of OR is 1, the result of EXOR is NOT A, and the result of NOR is 0.

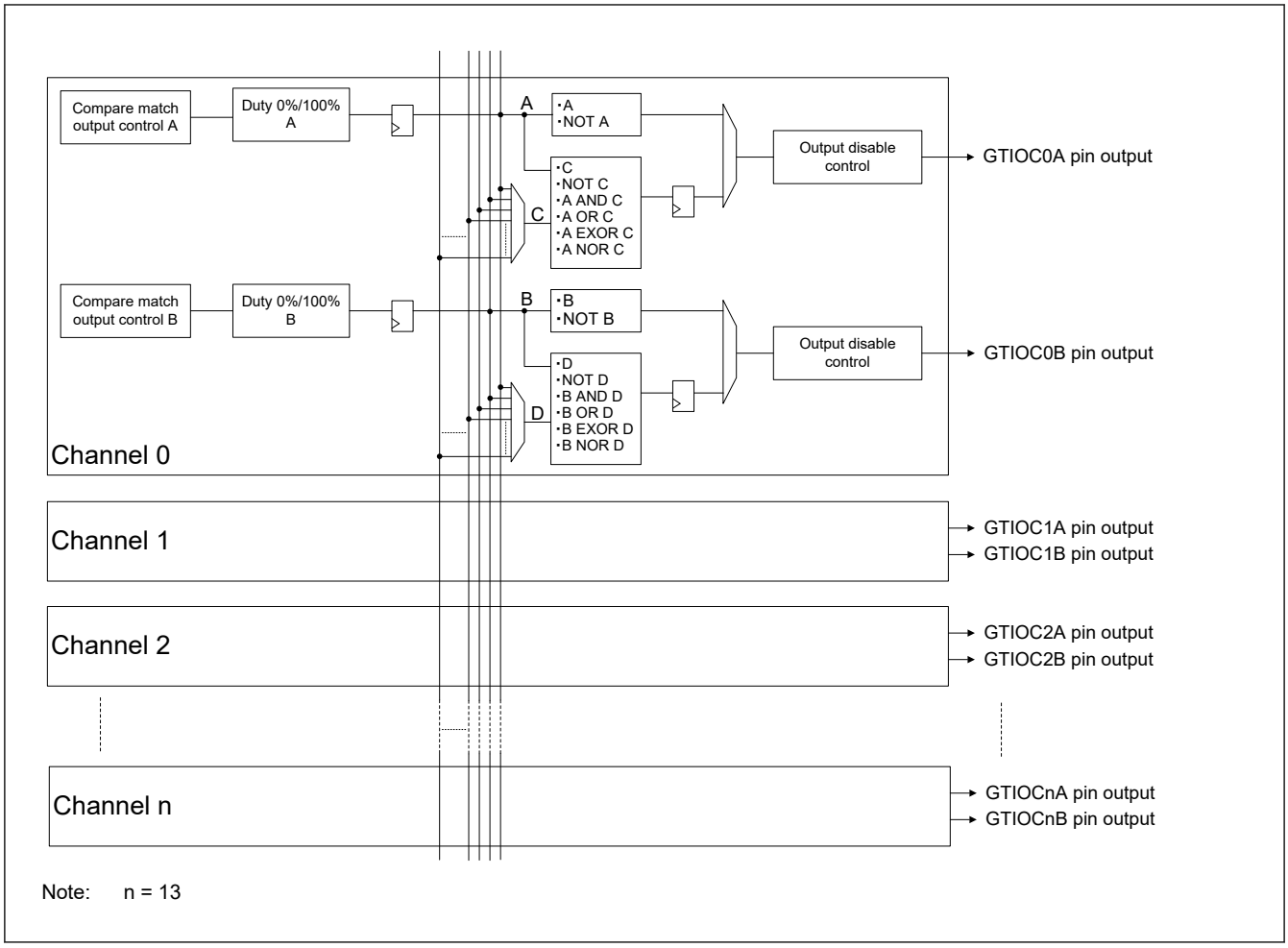


Figure 23.127 Block Diagram of Inter Channel Logical Operation

Figure 23.128 shows an example of inter channel logical operation.

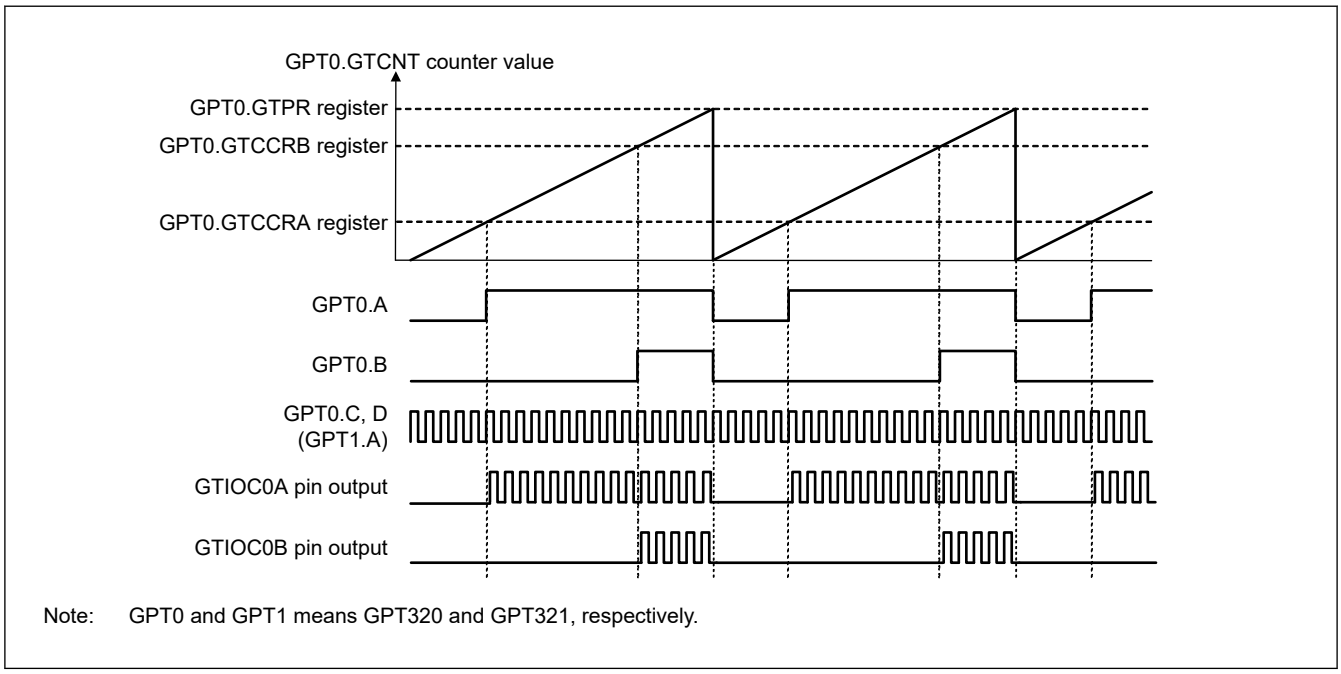


Figure 23.128 Example of Inter Channel Logical Operation

23.3.15 GTIOCnA/B Input/Output Pin Polarity Reversal Function

The polarity of the GTIOCnA, GTIOCnB input pins and the GTIOCnA, GTIOCnB output pins can be inverted according to the polarity of the external device.

When GTCR.AINV is “1”, the input and output of GTIOCnA are inverted. When GTCR.BINV is “1”, the input and output of GTIOCnB are inverted.

GTIOCnA and GTIOCnB are inverted at the final output stage immediately after input. When GTIOCnA and GTIOCnB are used as count start/stop/clear factors, countdown/up factors, and input capture factors, or when low/high/toggle output is used as PWM output, external input and external output are reversed. It is necessary to make settings that take this into consideration.

Set GTCR.AINV and BINV after setting the GTIOCnm pin functions during initial settings.

23.4 Interrupt Sources

23.4.1 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTADTR compare match
- GTCNT counter overflow (GTPR compare match)/underflow.
- period count function finish

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1, and an interrupt request is generated. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state. The Interrupt Controller Unit can change the relative channel priorities. However, the priority within a channel is fixed. For details, see section 14, Interrupt Controller Unit (ICU).

Table 23.71 lists the GPT interrupt sources.

Table 23.71 Interrupt sources

Channel	Name	Interrupt source	Interrupt flag	DTC activation
n = 0 to 13	GPTn_CCMPA	GPT32n.GTCCRA input capture/compare match	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT32n.GTCCRB input capture/compare match	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT32n.GTCCRC compare match	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT32n.GTCCRD compare match	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT32n.GTCCRE compare match	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT32n.GTCCRF compare match	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT32n.GTCNT overflow (GPT32n.GTPR compare match)	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT32n.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_PC	Period count function finish (n = 0 to 3, 10 to 13)	GTST[31] (PCF)	Possible

(1) GPTn_CCMPA interrupt (n = 0 to 13)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRA register
- When the GTCCRA register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRA register. In complementary PWM mode, GTCCRA register does not function as an input capture register.

(2) GPTn_CCMPB interrupt (n = 0 to 13)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register. In complementary PWM mode, GTCCRB register does not function as a compare match register.
- When the GTCCRB register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRB register. In complementary PWM mode, GTCCRB register does not function as an input capture register.

(3) GPTn_CMPC interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, GTCNT counter value of master channel) matches with the GTCCRC register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(4) GPTn_CMPD interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRD register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(5) GPTn_CMPE interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRE register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRE register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register).

(6) GPTn_CMPF interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRF register functions as a compare match register, the GTCNT counter value (in complementary PWM mode, the GTCNT counter value of master channel) matches with the GTCCRF register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[3:0] = 0001b (saw-wave one-shot pulse mode)
- GTCR.MD[3:0] = 0110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register).

(7) GPTn_OVF interrupt (n = 0 to 13)

An interrupt request is generated in the following conditions:

- In saw-wave PWM mode 1 and saw-wave one-shot pulse mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In saw-wave PWM mode 2, interrupt requests are enabled at overflows (GTCNT counter value changes from GTCCRm (m = A to F) register value selected with GTCSR.CSCMSC[2:0] bits to 0) or the time when GTCNT counter value matches GTPR register value.
- In triangle-wave mode, interrupt requests are enabled at crests (the GTCNT changes from GTPR to GTPR-1)
- In complementary PWM mode, interrupt requests are enabled at crests (GTCNT counter value of master channel changes from GTPR register value to GTPR register value minus 1).
- In counting by hardware sources (include external pulse width measuring function), an overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(8) GPTn_UDF interrupt (n = 0 to 13)

An interrupt request is generated in the following conditions.

- In saw-wave PWM mode 1 and saw-wave one-shot pulse mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (the GTCNT changes from 0 to 1)
- In complementary PWM mode, interrupt requests are enabled at troughs (GTCNT counter value of master channel changes from 0 to 1).
- In counting by hardware sources (include external pulse width measuring function), underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

About Interrupt signals and interrupt status flags, see section 23.2.16. GTST : General PWM Timer Status Register.

(9) GPTn_PC Interrupt (n = 0 to 3, 10 to 13)

When the GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1, an interrupt request is generated at the end of cycle.

23.4.2 DMAC and DTC Activation

The DMAC and DTC can be activated by the interrupt in each channel. For details, see section 14, Interrupt Controller Unit (ICU), section 17, DMA Controller (DMAC), and section 18, Data Transfer Controller (DTC).

23.4.3 Interrupt and A/D Conversion Start Request Skipping Function

23.4.3.1 Interrupt Skipping Function by GTITC Register

By setting the GTITC register, the GTCNT counter overflow (GTPR register compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF) can be skipped. Other interrupts and A/D conversion start request signals can be skipped in coordination with the GPTn_OVF/GPTn_UDF skipping function. When the interrupt is skipped, the updating of relevant status flag is also skipped. The interrupt skipping is continued even if the status flag is set to 1.

The interrupt skipping function is related only to the GTITC register setting, and is not related to setting of the GTINTAD register interrupt enable bit. The interrupt skipping is continued even if the interrupt is disabled with GTINTAD register setting.

When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times of skipping is odd, GPTn_OVF/GPTn_UDF interrupt requests cannot be generated at troughs only or at crests only depending on the skipping counter start timing. Therefore, in order to count both troughs and crests and generate the GPTn_OVF/GPTn_UDF interrupts at troughs only or crests only in triangle-wave mode, the number of times of skipping should be even.

Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GPTn_OVF/GPTn_UDF interrupt requests are sometimes not generated at overflows only or at underflows only. Therefore, in order to count both overflows and underflows with the count direction changed and generate the GPTn_OVF/GPTn_UDF interrupts at overflows only or underflows only in saw-wave mode, the skipping state should be carefully checked before using.

When changing the skipping count, be sure to release the skipping count setting (GTITC.IVTC[1:0] bits = 00b).

Figure 23.129 to Figure 23.134 show examples of skipping function operation.

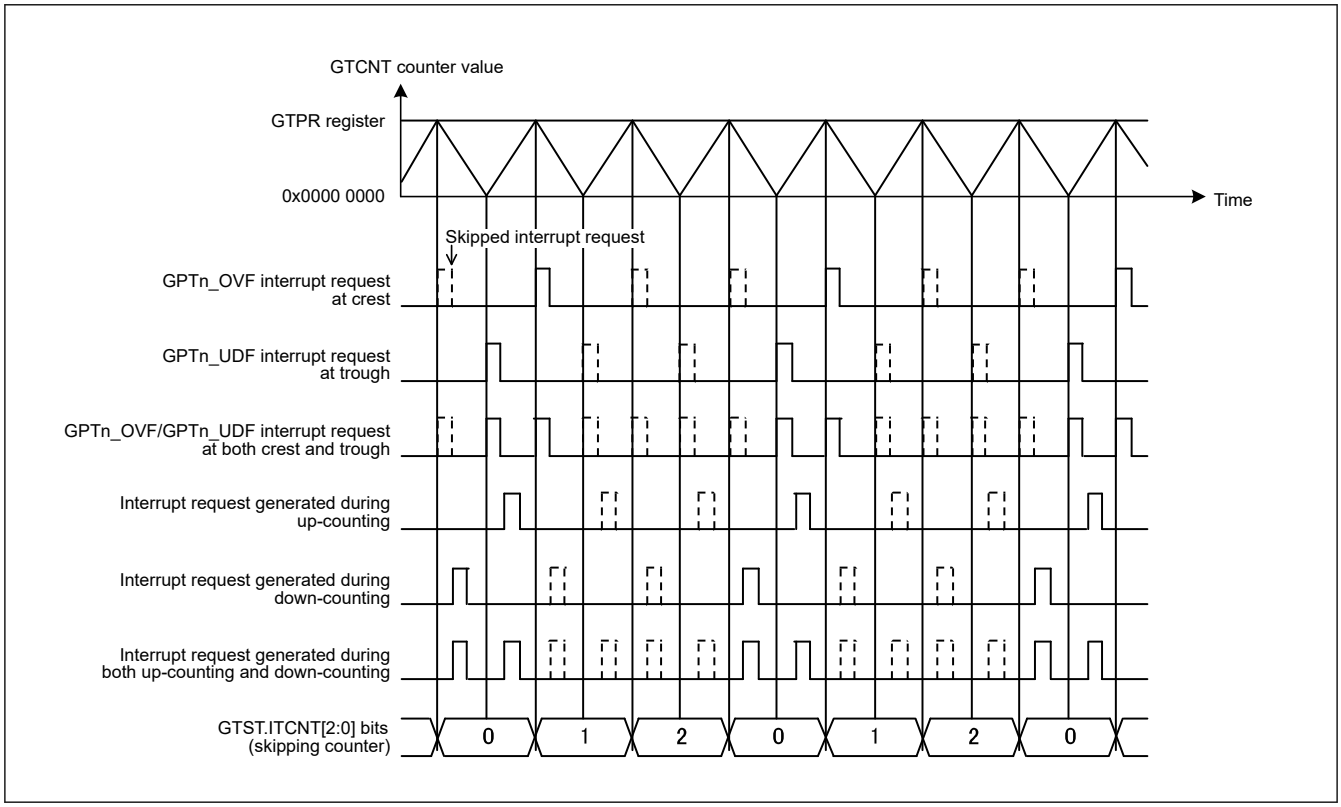


Figure 23.129 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Crests, Skipping Count: 2)

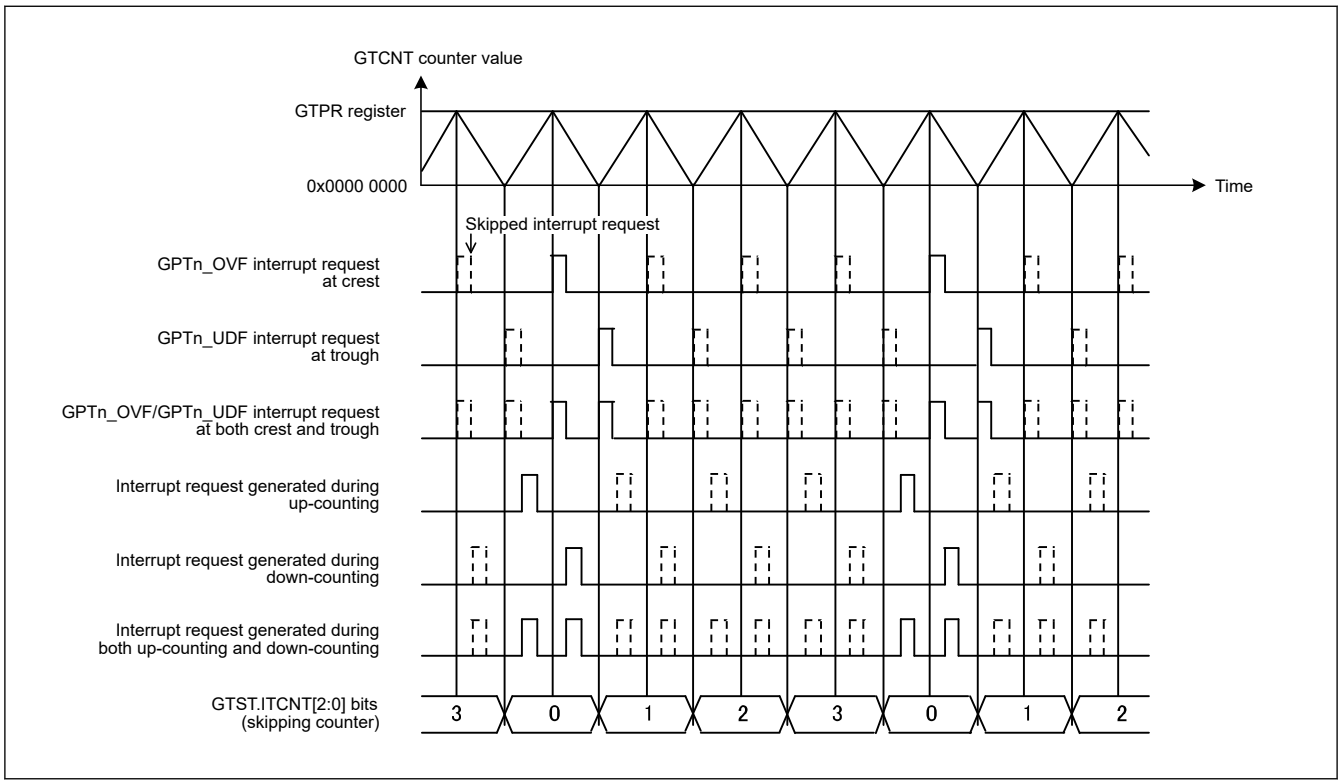


Figure 23.130 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Troughs, Skipping Count: 3)

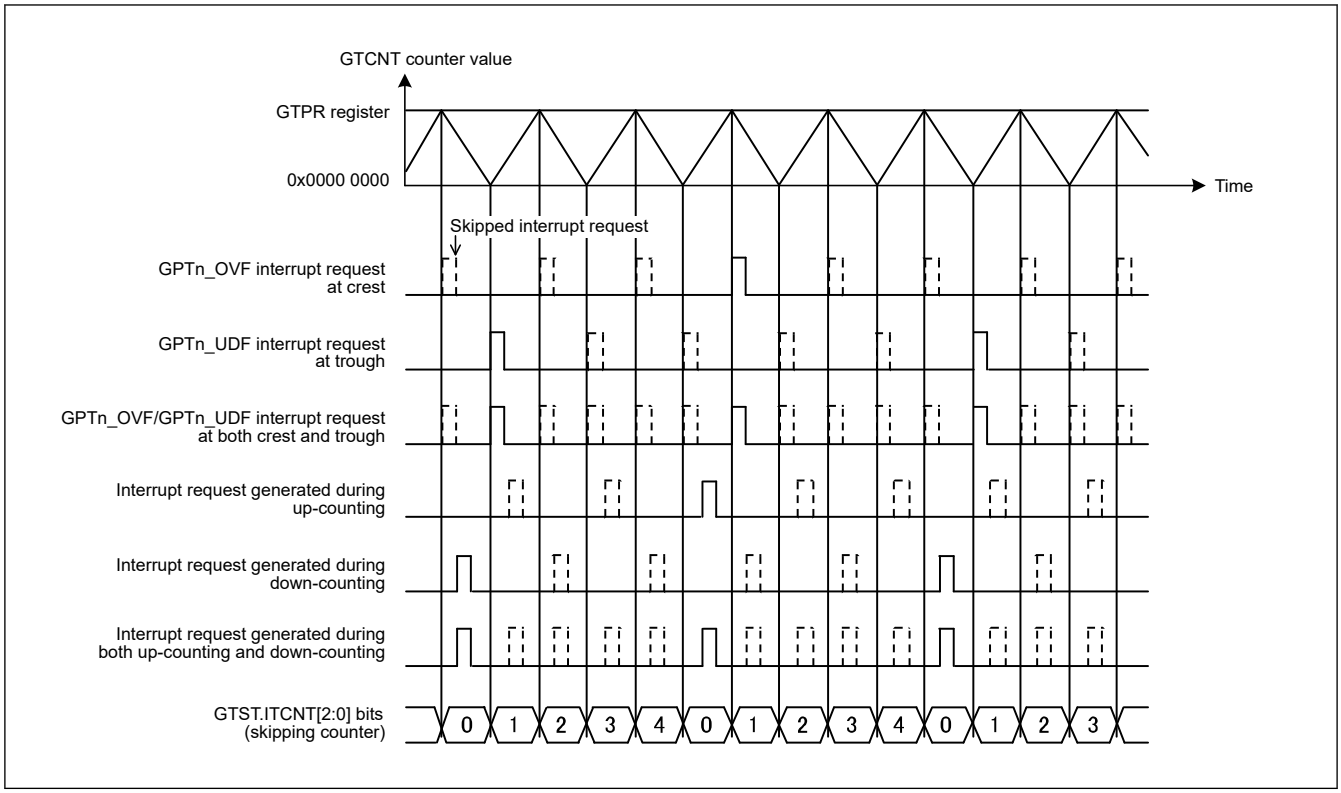


Figure 23.131 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 4)

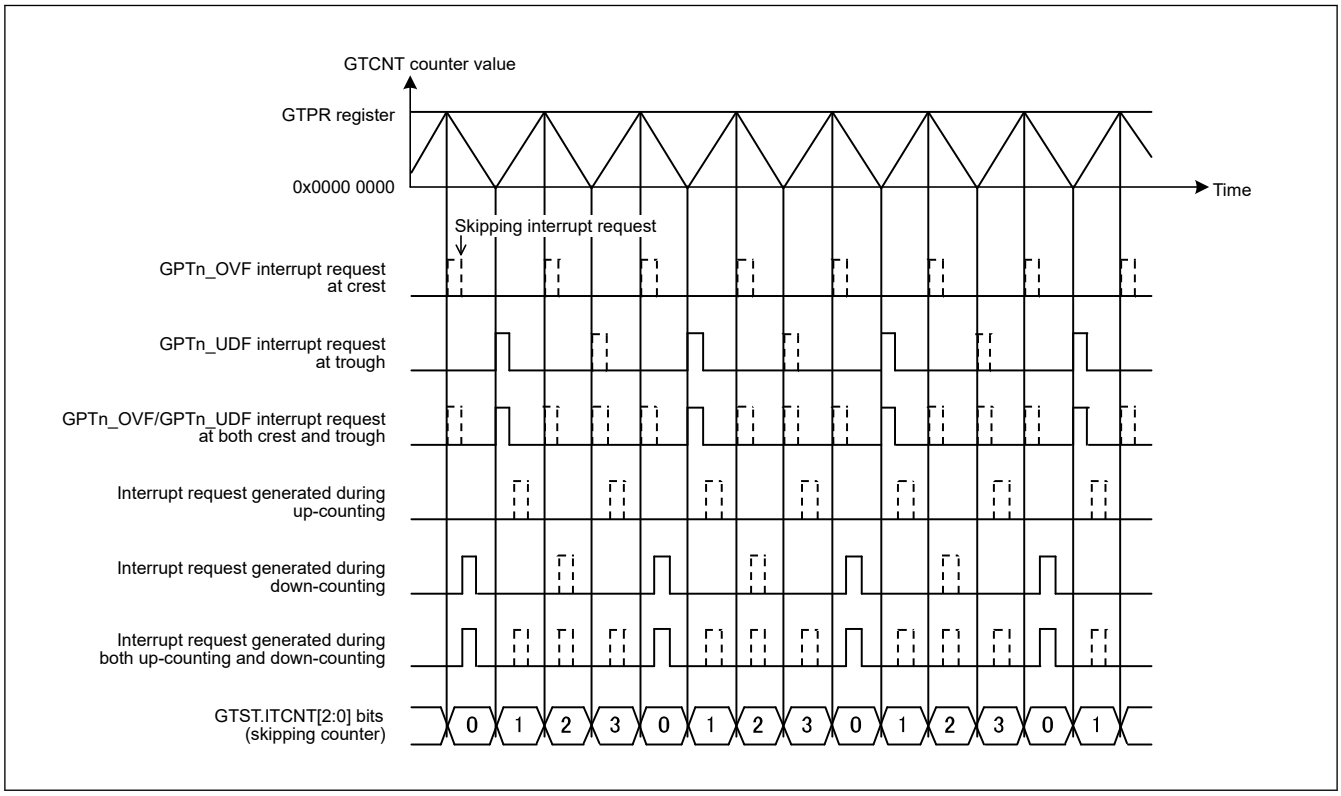


Figure 23.132 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Up-Counting)

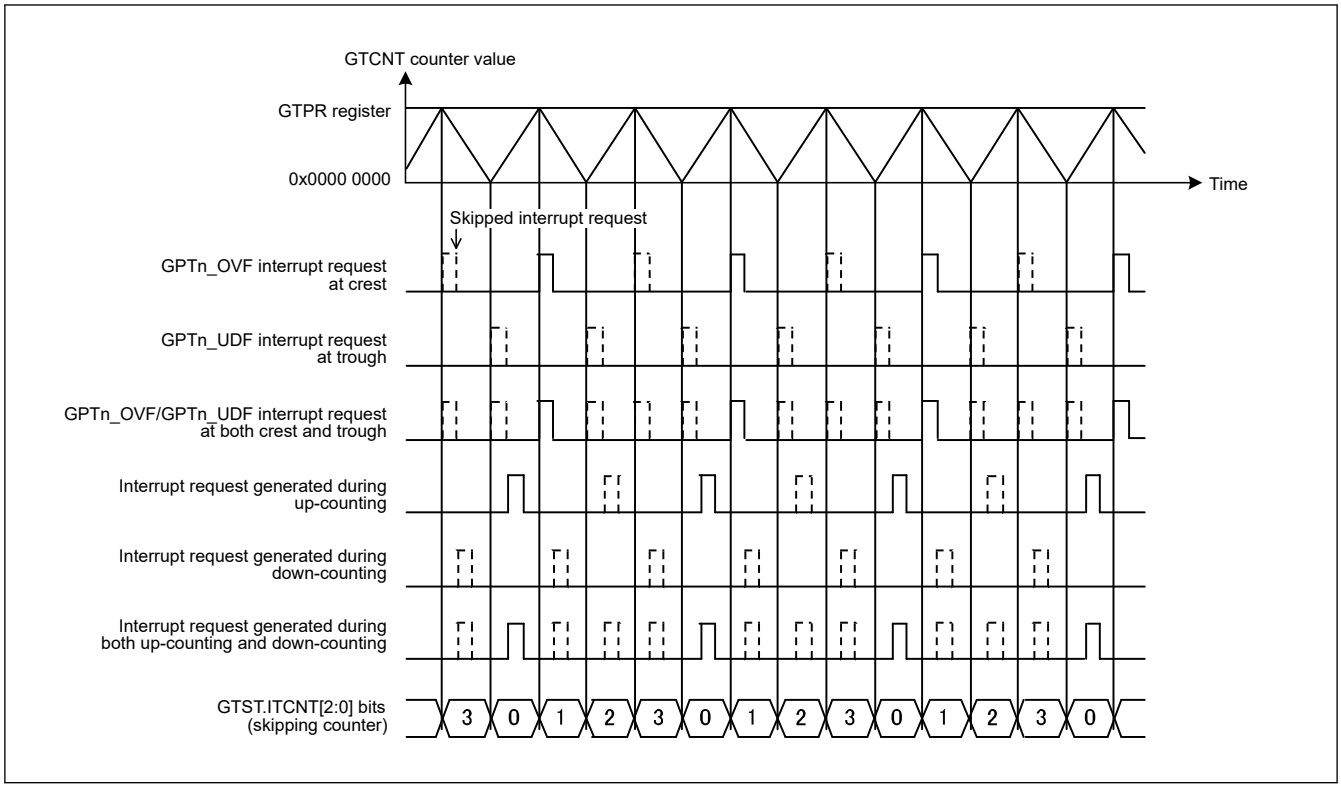


Figure 23.133 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Down-Counting)

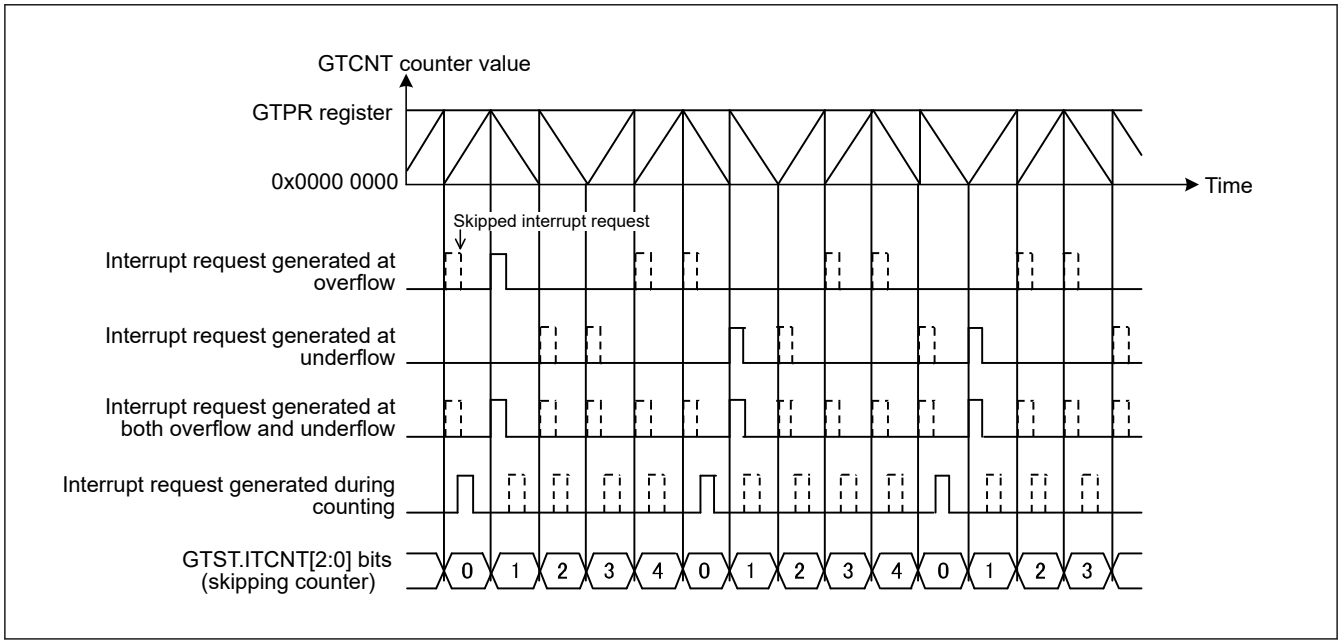


Figure 23.134 Example of Interrupt Skipping Function Operation (Saw Waves, Operation with Count Direction Changed, Counting and Skipping Both Overflows and Underflows, Skipping Count: 4)

23.4.3.2 Extended Interrupt Skipping Function

Overflow/underflow interrupt, compare match/input capture interrupt, A/D conversion start request, and buffer transfer can be skipped by counting the GTCNT counter overflow or underflow based on settings of the GTEITC, GTEITLI1, GTEITLI2 and GTEITLB registers.

Overflow/underflow interrupt, compare match/input capture interrupt, A/D conversion start request, and buffer transfer can individually be set for skipping and the skipping period using the GTEITLI1, GTEITLI2, and GTEITLB registers.

The skipping period is set, related to the operation of the two independent extended interrupt skipping counters (EITCNT1[3:0] and EITCNT2[3:0] bits in the GTEITC registers), as a period that either of the counter value for such skipping counters is other than 0 or other than the skipping count. The skipping period can also be set as a period that the both skipping counters are set as other than 0 or other than the skipping count for the counter value.

Figure 23.135 shows the counter operation for interrupt skipping by the GTITC register and extended interrupt skipping.

The counter operation for extended interrupt skipping is set by the GTEITC register.

The EITCNT1[3:0] bits are set for 0 as initial value and then they count the count source (in Figure 23.135, a crest is selected) selected by the extended interrupt counter 1 count source select bit (GTEITC.EIVTC1[1:0] bits), and repeat the count operation which returns to 0 when the skipping count (in Figure 23.135, count is 2) set by the extended interrupt skipping 1 skipping count setting bit (EIVTT1[3:0] bits) is achieved.

The EITCNT2[3:0] bits can be set for the initial value and they count the count source (in Figure 23.135, a trough is selected) selected by the extended interrupt counter 2 count source select bit (EIVTC2[1:0] bits), and repeat the count operation which return to 0 when the skipping count (in Figure 23.135 count is 2) set by the EIVTT2[3:0] bits is achieved. The initial value is set when the GTEITC register is written by the access of upper 16 bits or 32 bits while the setting for the extended interrupt skipping counter 2 is not counted (EIVTC2[1:0] bits are 00b) and when the write value to the EIVTC2[1:0] bits is other than 00b. When the initial value is set, the write value to the extended interrupt skipping counter 2 initial value bits (EITCNT2IV[3:0] bits) are set as the initial value for the EITCNT2[3:0] bits.

The extended interrupt skipping counter starts up-counting at the first count clock after the setting is modified from not counting to counting.

The interrupt skipping count counter (GTST.ITCNT[2:0] bits) for the interrupt skipping function set by the GTITC register is reset to 000b when the GTCNT counter operation is stopped: however, the EITCNT1[3:0] and EITCNT2[3:0] bits for the extended interrupt skipping function retain the value even after the GTCNT counter operation is stopped, and the counting can be resumed from the value before the counter is stopped. When values for the EITCNT1[3:0] and EITCNT2[3:0] bits are to be reset (0000b), set the EIVTC1[1:0] and EIVTC2[1:0] bits to the setting for not counting (not skipping) (00b).

When the skipping count is to be changed, change the count after stopping the skipping counter operation (set either of the EIVTC1[1:0] bit or the EIVTC2[1:0] bit to 00b).

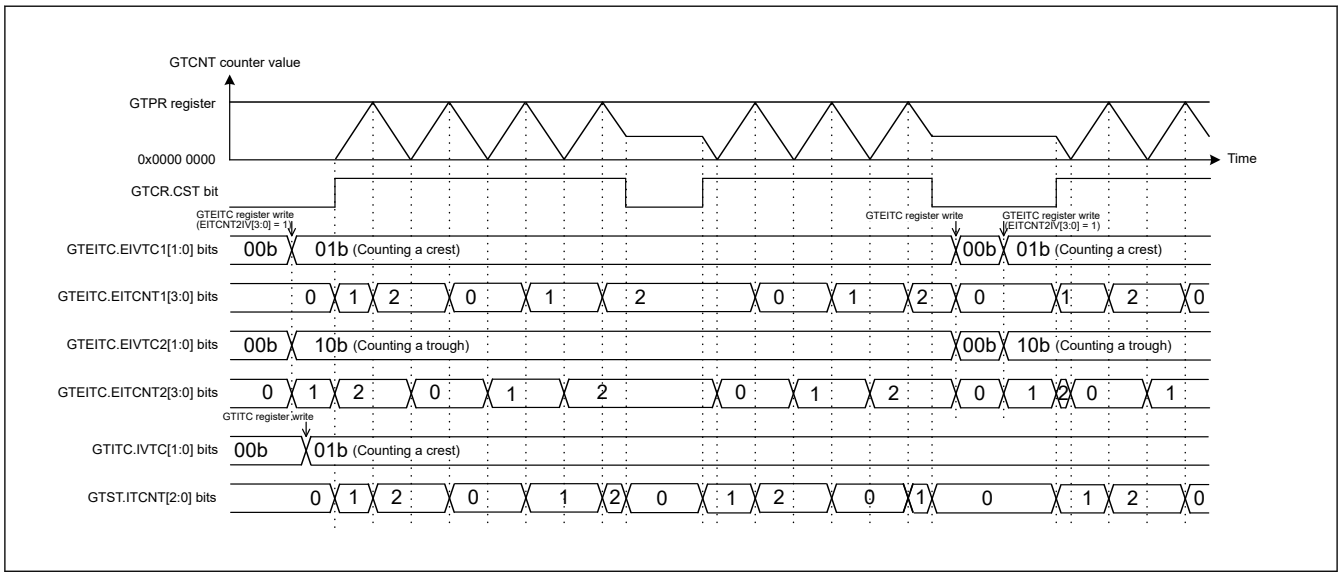


Figure 23.135 Example of Counter Operation for Interrupt Skipping

Interrupt skipping by the GTEITL1 register and A/D conversion start request skipping by the GTEITLI2 register can be performed simultaneously with skipping by the GTITC register or GTADCMSC register. A skipping period in this case is represented by OR-ed skipping periods of respective registers.

Figure 23.136 shows corresponding interrupt skipping operations by different registers are performed simultaneously.

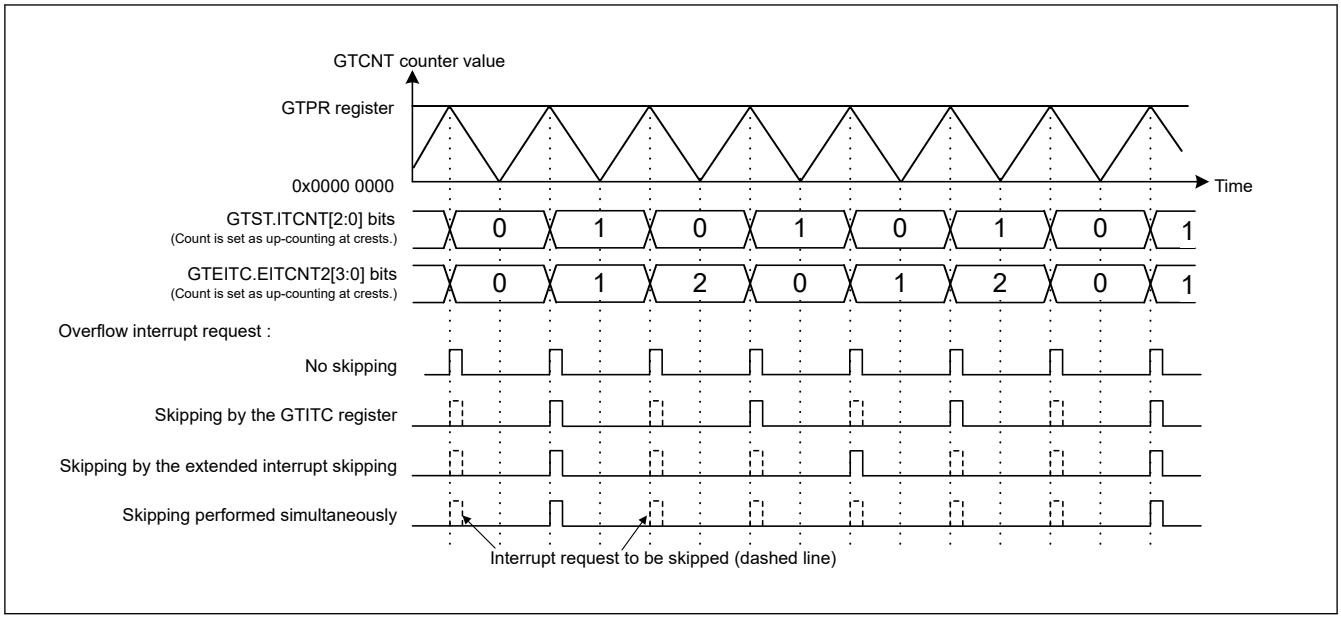


Figure 23.136 Example of Interrupt Skipping Operation (Skipping by the GTITC Register: Counting crests, Extended Interrupt Skipping: EIVTC1[1:0] bits = 00b, EIVTC2[1:0] bits = 01b, EITLV[2:0] bits = 010b)

When the extended interrupt skipping selected by GTEITLI1 is performed, the relevant status flag is also skipped. The skipping function is continued even if the status flag is set to 1.

When A/D conversion start request skipping selected by GTEITLI2 is performed, the relevant status flag is also skipped. The skipping function is continued even if the status flag is set to 1.

Skipping of updating of status flag and ELC event source outputs corresponding to A/D conversion start request for which skipping can be set up in the GTEITLI2 register is only based on the settings of the GTITC register and the extended interrupt skipping register, and has no connection with the setting of A/D conversion start request enable bit in the GTINTAD register. The A/D conversion start request enable bit is used only for A/D conversion start request output(ELC event source output) after skipping.

A buffer transfer skipping by the GTEITLB register is performed in all of the buffer operations which is enabled in the GTBER and GTDTCR registers and GTBER2 register, or all buffer operations performed by saw-wave one-shot pulse mode or triangle-wave PWM mode 3 or complementary PWM mode (excludes buffer transfer from GTCCRC, GTCCRE to GTCCRA).

An interrupt skipping and a buffer transfer skipping are operated individually. An interrupt output without performing a buffer transfer and performing a buffer transfer without an interrupt output can also be operated.

Figure 23.137 to Figure 23.144 show examples of extended skipping function operation.

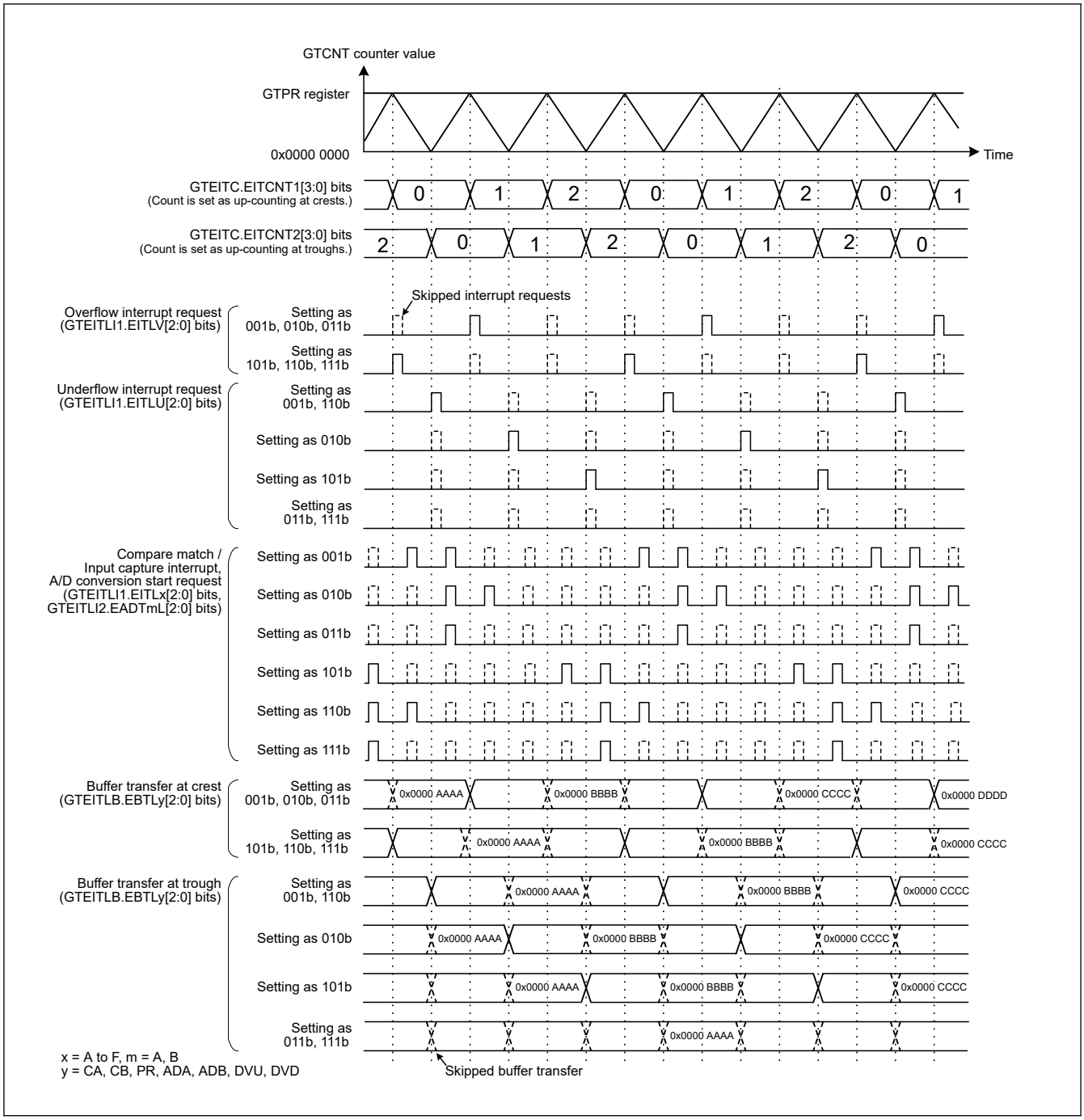


Figure 23.137 Example of Extended Interrupt Skipping Function (Triangle wave, Counting Crests, Extended Interrupt Skipping 1 Skipping Count: 2, Counting Troughs, Extended Interrupt Skipping 2 Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 0)

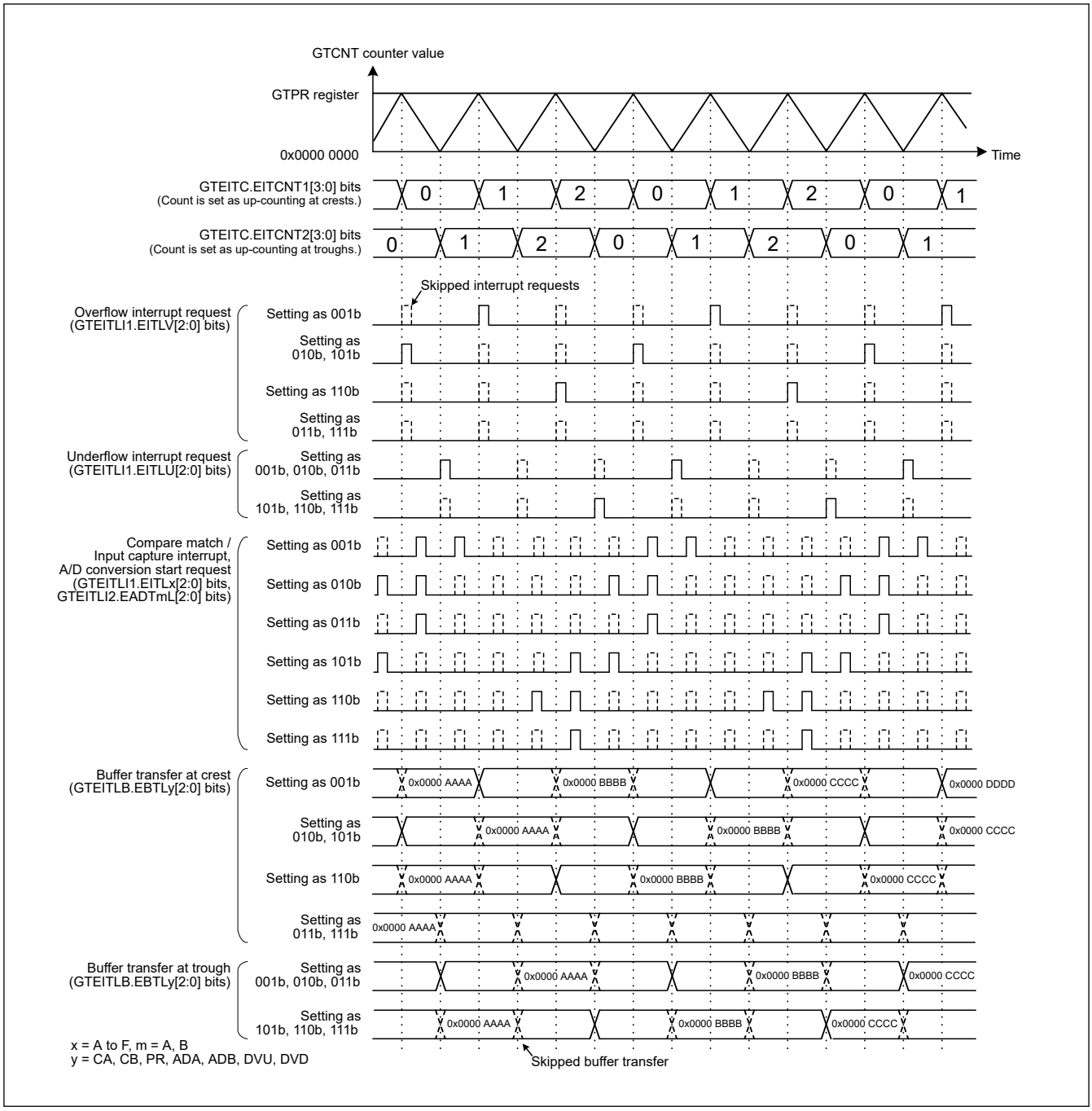


Figure 23.138 Example of Extended Interrupt Skipping Function (Triangle Waves, Count Crests by the Extended Interrupt Skipping 1 with Skipping Count: 2, Count Troughs by the Extended Interrupt Skipping 2 with Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 1)

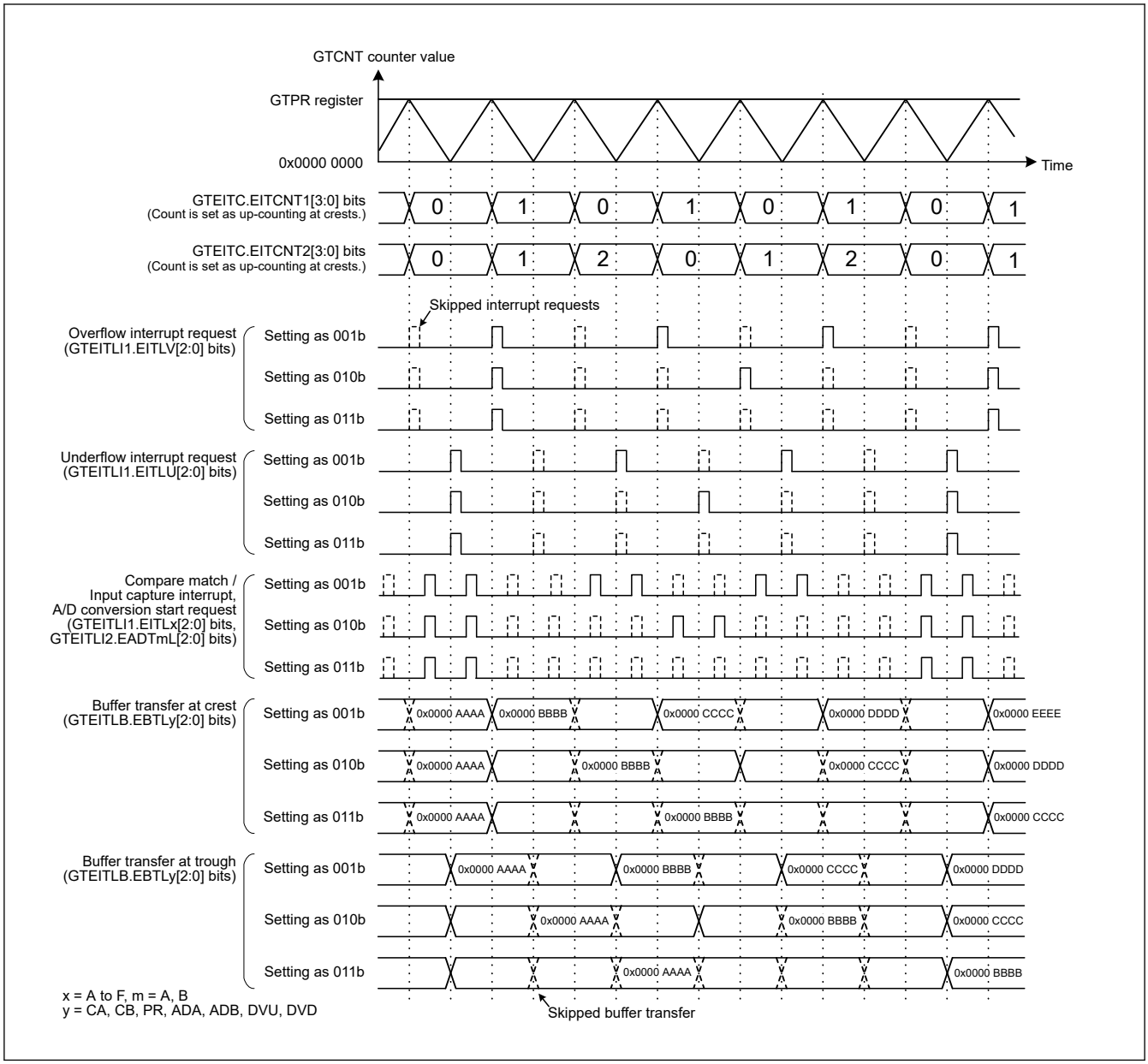


Figure 23.139 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting Crests, Extended Interrupt Skipping 1 Skipping Count: 1, Counting Crests, Extended Interrupt Skipping 2 Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as 0)

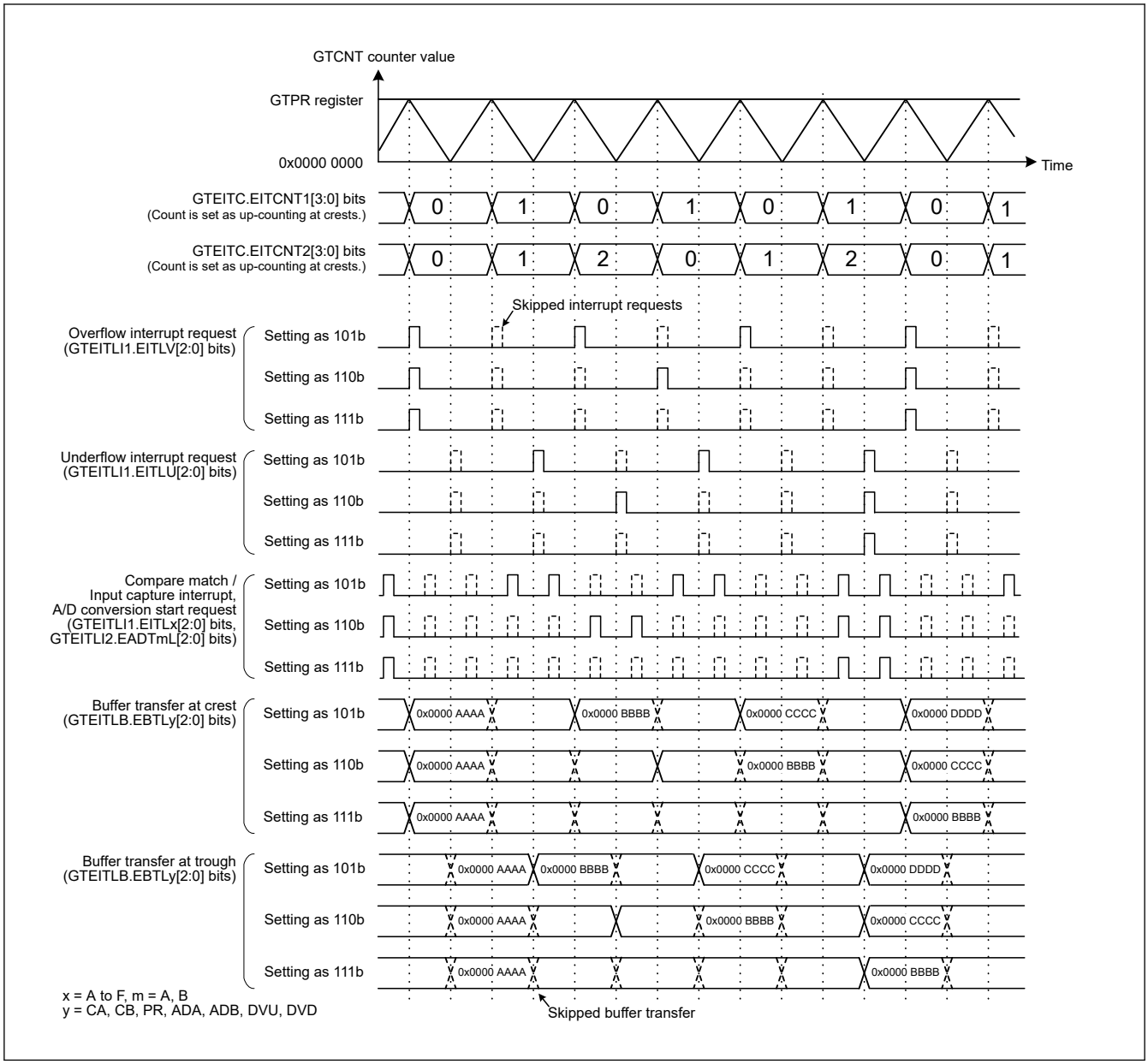


Figure 23.140 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting Crests, Extended Interrupt Skipping 1 Skipping Count: 1, Counting Crests, Extended Interrupt Skipping 2 Skipping Count: 2, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as GTEITC.EIVTTk bits.)

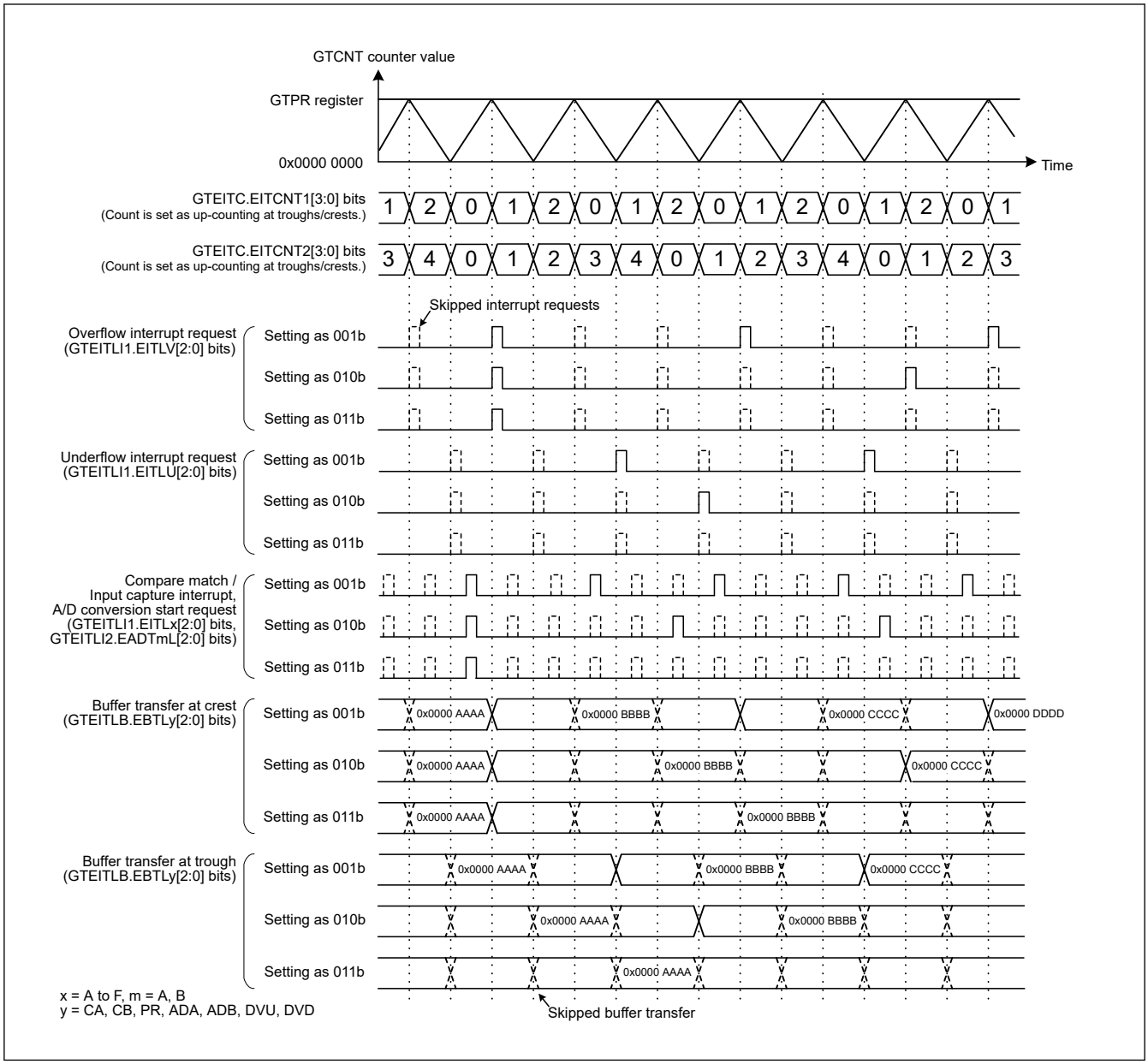


Figure 23.141 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting both Crests and Troughs, Extended Interrupt Skipping 1 Skipping Count: 2, Counting both Crests and Troughs, Extended Interrupt Skipping 2 Skipping Count: 4, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as 0)

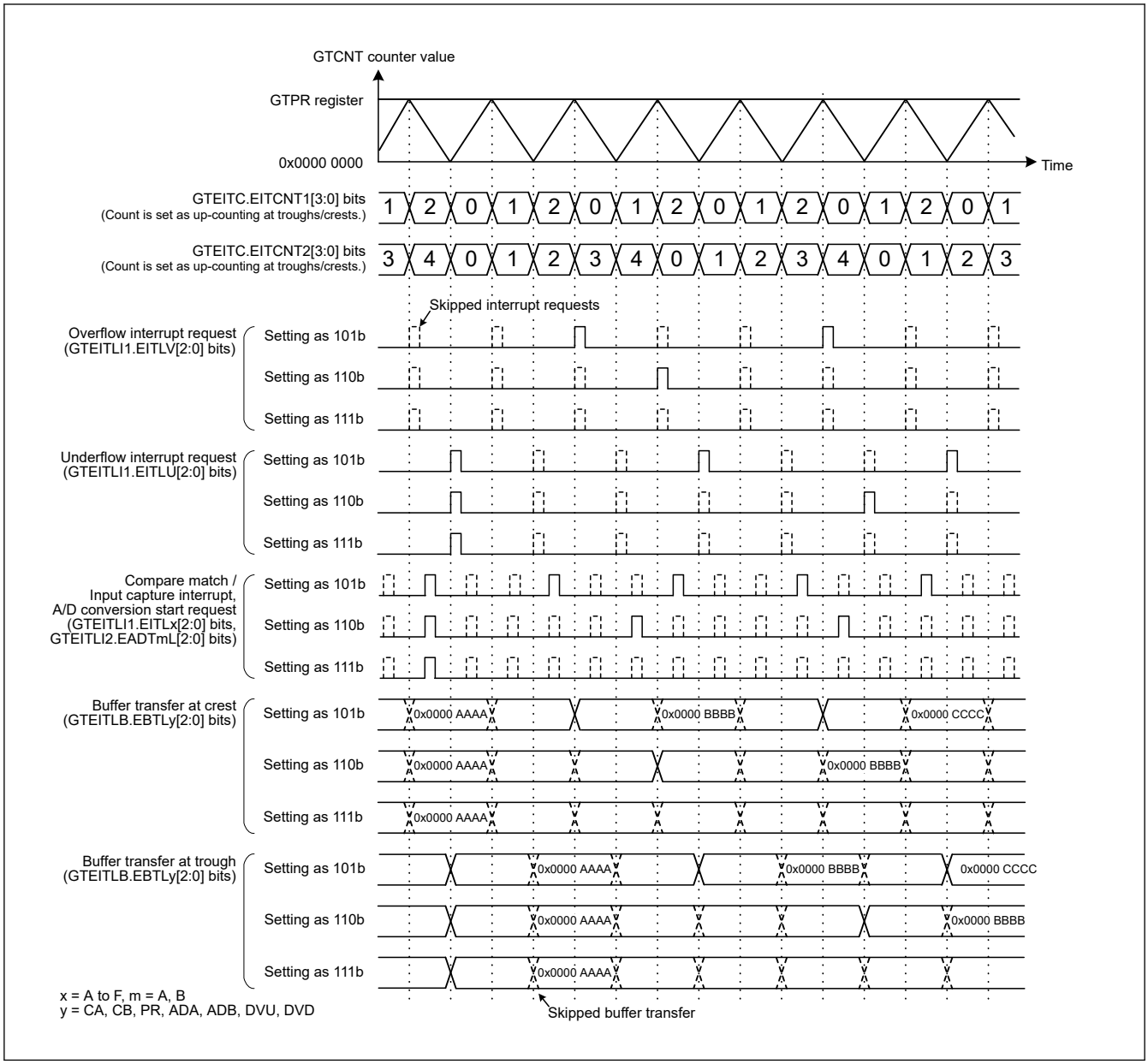


Figure 23.142 Example of Extended Interrupt Skipping Function Operation (Triangle Waves, Counting both Crests and Troughs, Extended Interrupt Skipping 1 Skipping Count: 2, Counting both Crests and Troughs, Extended Interrupt Skipping 2 Skipping Count: 4, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as GTEITC.EIVTTk bit.)

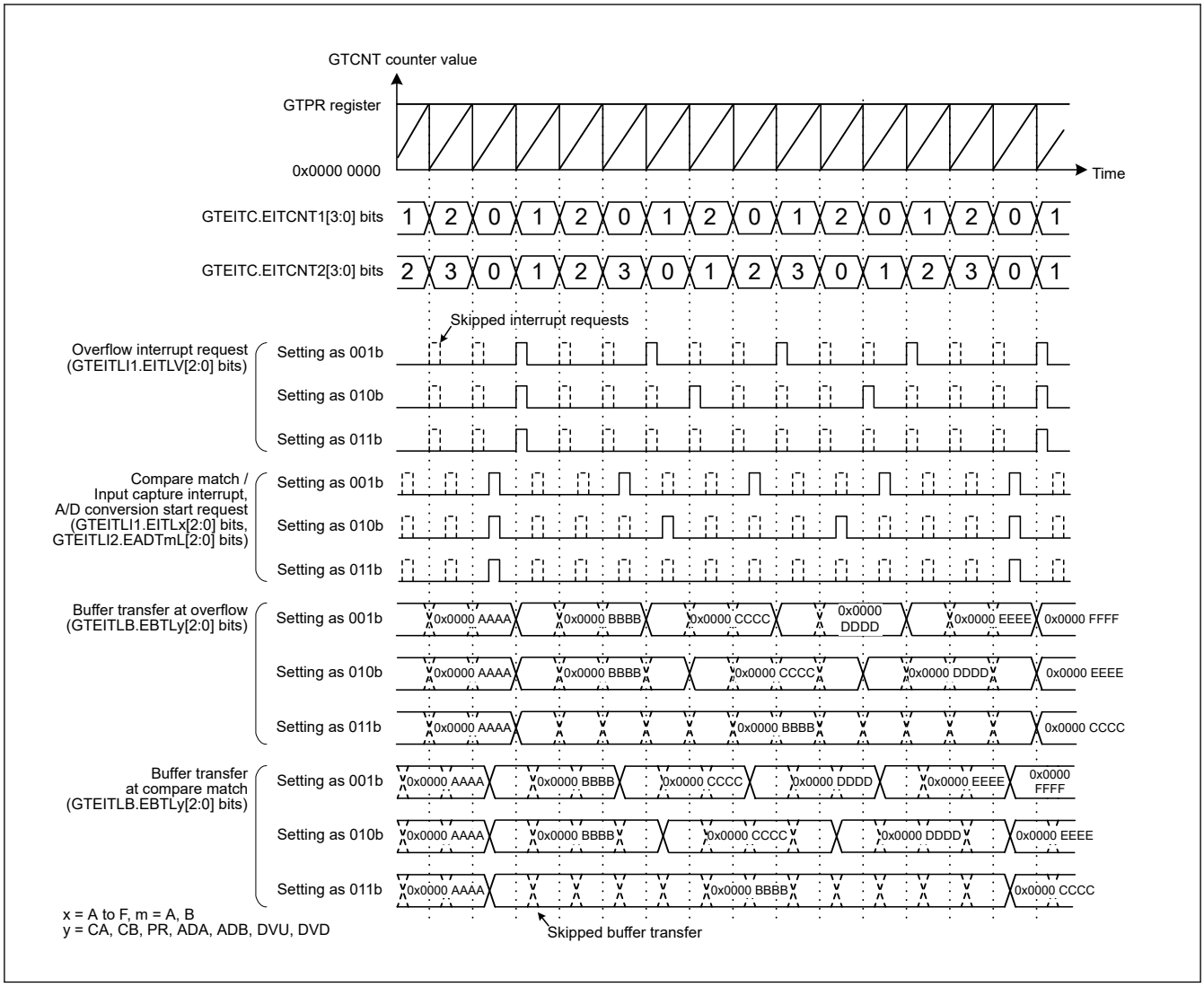


Figure 23.143 Example of Extended Interrupt Skipping Function Operation (Up-Counting in Saw Waves, Counting Overflow, Extended Interrupt Skipping 1 Skipping Count: 2, Counting Overflow, Extended Interrupt Skipping 2 Skipping Count: 3, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as 0)

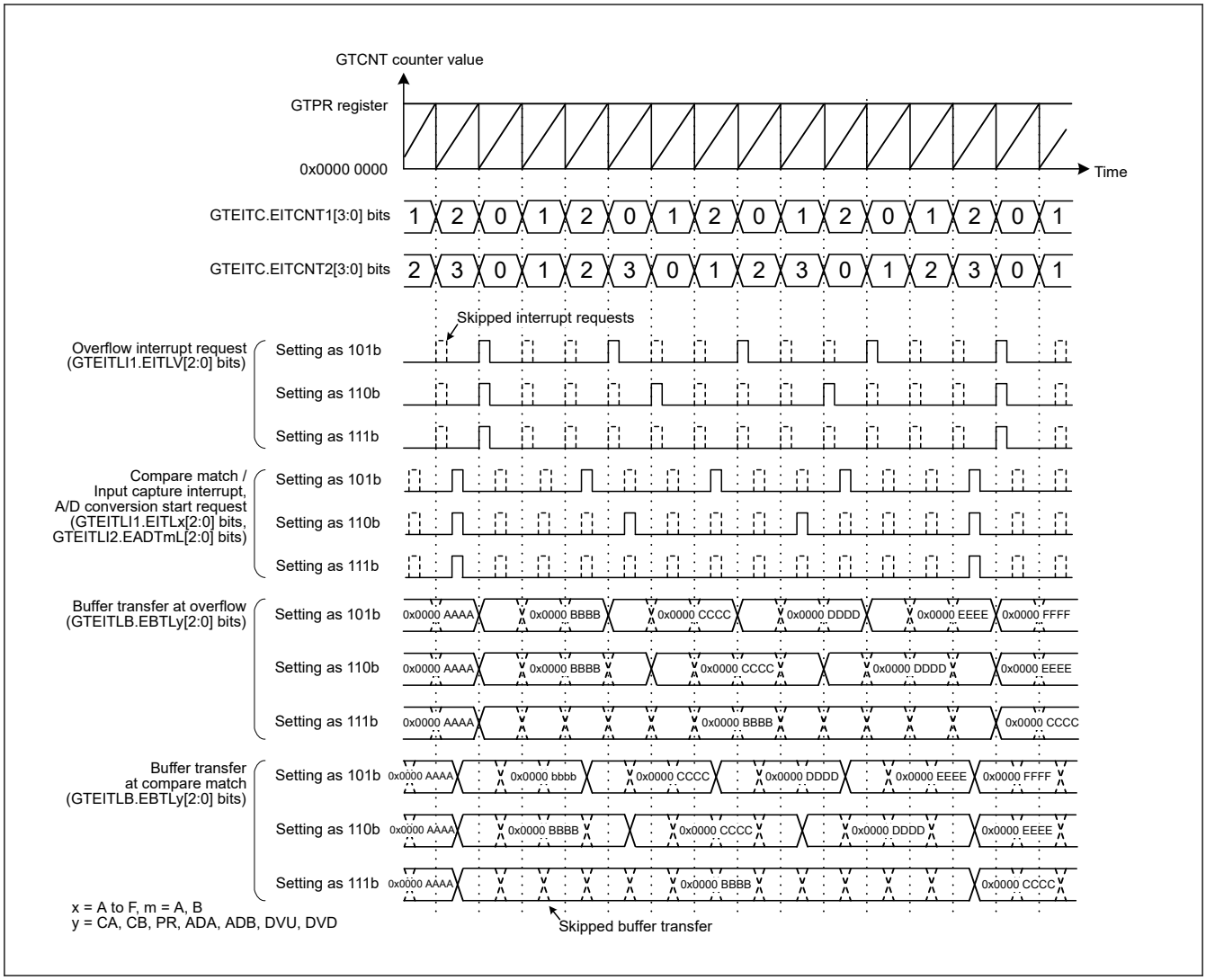


Figure 23.144 Example of Extended Interrupt Skipping Function Operation (Up-Counting Saw Waves, Counting Overflow, Extended Interrupt Skipping 1 Skipping Count: 2, Counting Overflow, Extended Interrupt Skipping 2 Skipping Count: 3, Extended Interrupt Skipping Counter 2 Initial Value: 0, Skipped in the Period other than GTEITC.EITCNTk bits (k = 1, 2) as GTEITC.EIVTTk bits.)

Figure 23.145 shows an example of the extended interrupt skipping operation on the input capture. When the setting is for the input capture operation setting (GTCR.ICDS bit = 0) at count stop of the GTCNT counter, the interrupt by the input capture and the extended skipping on buffer transfer is enabled even at count stop of the GTCNT counter.

When the input capture is generated at count stop of the GTCNT counter by setting the ICDS bit as 0, an interrupt and a buffer transfer are skipped if the skipping counter value is the same with the skipping period set in a corresponding interrupt skipping function select bit.

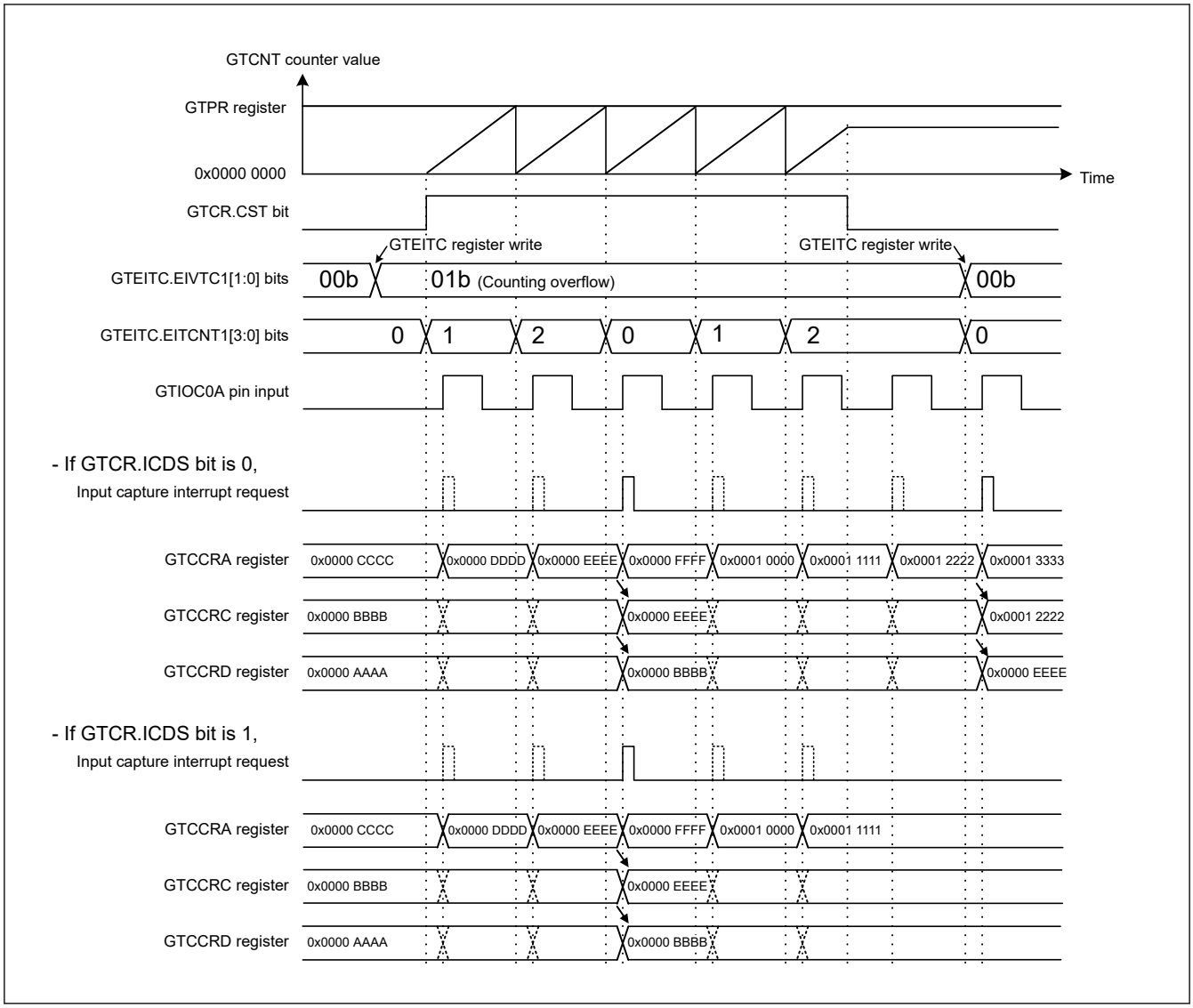


Figure 23.145 Example of Input Capture Operation in the Extended Interrupt Skipping Function Operation (Up-Counting Saw Waves, Counting Overflow, Extended Interrupt Skipping 1 Skipping Count: 2, Skipped in the Period other than the EITCNT1 as 0, Input Capture at the Input Rising)

Table 23.72 shows an example of setting the extended interrupt skipping.

The extended interrupt skipping counter 2 initial value is set by the written value to the ETICNT2IV[3:0] bits which is applied to change the setting from not counting the extended interrupt skipping counter 2 count source (GTEITC.EIVTC2[1:0] bits = 00b) to counting (EIVTC2[1:0] bits = other than 00b). Writing to the extended interrupt skipping counter 2 initial value bit (ETICNT2IV[3:0] bits) is performed only when the setting of the above-mentioned extended interrupt skipping counter 2 initial value is written.

Table 23.72 Example for Setting the Extended Interrupt Skipping (1 of 2)

No.	Step Name	Description
1	Set GTCNT counter operation, Set buffer operation, Set compare match value	See section 23.3.2. Buffer Operation, section 23.3.3. PWM Output Operating Mode, and so on.
2	Set the extended interrupt skipping function	Select the skipping counter used for skipping and the skipping period with the skipping function select bit for the interrupt, for the A/D conversion start request, and for a buffer transfer, all which are to be skipped, in the GTEITLI1, GTEITLI2, and GTEITLB registers respectively.

Table 23.72 Example for Setting the Extended Interrupt Skipping (2 of 2)

No.	Step Name	Description
3	Set the extended skipping counter	With the GTEITC register, set a count source of the skipping counter used for skipping, skipping count, and the skipping counter 2 initial value as the following order. Set EIVTCk[1:0] bits (k = 1,2) as value other than 00b, and set EIVTTk[3:0] bits as value other than 0000b. When the skipping counter 2 is used, change EIVTC2[1:0] bits from 00b to value other than 00b as well as set EITCNT2IV[3:0] bits to the skipping counter 2 initial value.
4	Start count operation	Set GTCR.CST to 1 to start count operation.
5	Set buffer value for each cycle	See section 23.3.2. Buffer Operation, section 23.3.3. PWM Output Operating Mode, and so on.

23.4.3.3 A/D conversion Start Request Compare Match Skipping Function

The A/D conversion start request and GTADTR register buffer transfer can be skipped by counting the compare matches of GTADTRA register and GTADTRB register based on settings of the GTADCMSC register and GTADCMSS register.

The skipping period is set, related to the operation of the two independent A/D conversion start request compare match skipping counters (ADCMSCNT1[3:0] and ADCMSCNT2[3:0] bits in the GTADCMSC register), as a period that either of the counter value for such skipping counters is other than 0 or other than the skipping count. The skipping period can also be set as a period that the both skipping counters are set as other than 0 or other than the skipping count for the counter value.

Figure 23.146 shows the counter operation for A/D conversion start request compare match skipping.

The counter operation for A/D conversion start request compare match skipping is set by the GTADCMSC register.

The ADCMSCNT1[3:0] bits count the count source (in Figure 23.146, a crest is selected) selected by the A/D conversion start request compare match skipping counter 1 count source select bit (GTADCMSC.ADCMSC1[1:0] bits), and repeat the count operation which returns to 0 when the skipping count (in Figure 23.146, count is 2) set by the A/D conversion start request compare match skipping 1 skipping count setting bit (ADCMST1[3:0] bits) is achieved.

The ADCMSCNT2[3:0] bits count the count source (in Figure 23.146, a trough is selected) selected by the A/D conversion start request compare match skipping counter 2 count source select bit (GTADCMSC.ADCMSC2[1:0] bits), and repeat the count operation which returns to 0 when the skipping count (in Figure 23.146, count is 2) set by the A/D conversion start request compare match skipping 2 skipping count setting bit (ADCMST2[3:0] bits) is achieved.

The ADCMSCNTk[3:0] bits (k = 1, 2) can be set for the initial value. The initial value is set when the GTADCMSC register is written by the access of 16 bits or 32 bits while the setting for the A/D conversion start request compare match skipping counter k is not counted (ADCMSCk [1:0] bits are 00b) and the write value to the ADCMSCk[1:0] bits is other than 00b. When the initial value is set, the write value to the A/D conversion start request compare match skipping counter k initial value bits (ADCMSCNTkIV[3:0] bits) are set as the initial value for the ADCMSCNT2[3:0] bits.

The A/D conversion start request compare match skipping counter starts up-counting at the first count clock after the setting is modified from not counting to counting.

The ADCMSCNT1[3:0] and ADCMSCNT2[3:0] bits for the A/D conversion start request compare match skipping function retain the value even after the GTCNT counter operation is stopped, and the counting can be resumed from the value before the counter is stopped. When values for the ADCMSCNT1[3:0] and ADCMSCNT2[3:0] bits are to be reset (0000b), set the ADCMSC1[1:0] and ADCMSC2[1:0] bits to the setting for not counting (not skipping) (00b).

When the skipping count is to be changed, change the count after stopping the skipping counter operation (set either of the ADCMSC1[1:0] bit or the ADCMSC 2[1:0] bit to 00b).

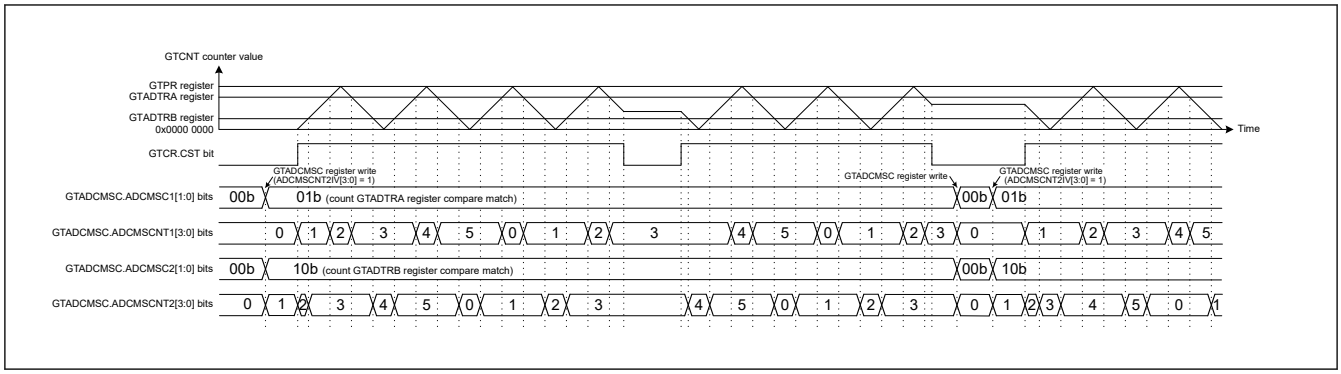


Figure 23.146 Example of A/D Conversion Start Request Compare Match Skipping Function Operation

A/D conversion start request skipping by the ADCMSC register can be performed simultaneously with skipping by the GTITC register or GTEITC register. A skipping period in this case is represented by OR-ed skipping periods of respective registers.

Figure 23.147 shows corresponding interrupt skipping operations and A/D conversion start request skipping operation are performed simultaneously.

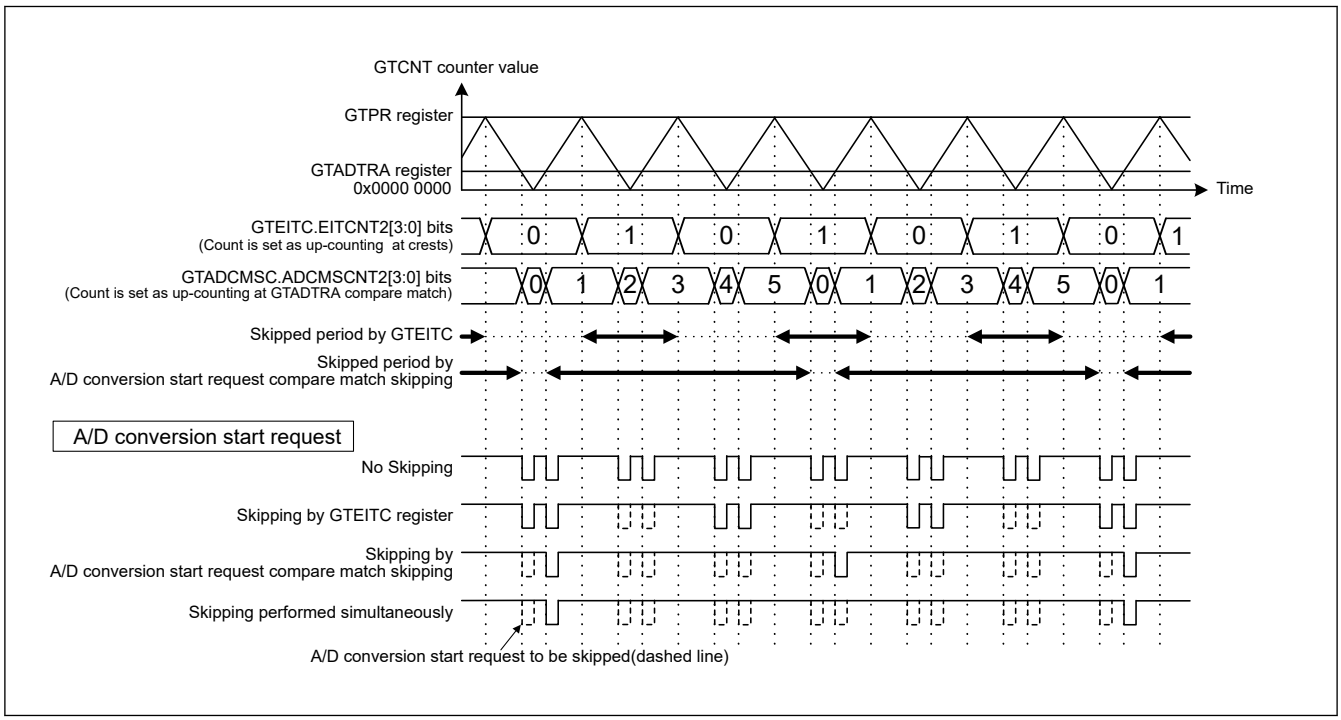


Figure 23.147 Example of A/D Conversion Start Request Compare Match Skipping Function Operation (Extended Interrupt Skipping: EIVTC2[1:0] = 01b, EADTAL[2:0] = 010b, A/D Conversion Start Request Compare Match Skipping: ADCMSC2[1:0] = 01b, ADCMSAL[2:0] = 010b)

When A/D conversion start request skipping which can be set by the GTADCMSS register is performed, updating of status flag and the ELC event output depend on the A/D conversion start request enable bit in the GTINTAD register. All the operations by A/D conversion start request which are set as disable by the GTINTAD register is not performed.

A buffer transfer skipping by the GTADCMSS register is performed in all of the buffer operations which is enabled in the GTBER and GTBER2 register, or all buffer operations performed by saw-wave one-shot pulse mode or triangle-wave PWM mode 3 or complementary PWM mode (excludes buffer transfer from GTCCRC, GTCCRE to GTCCRA).

An A/D conversion start request skipping and a buffer transfer skipping are operated individually.

Figure 23.148, Figure 23.149 show examples of extended skipping function operation.

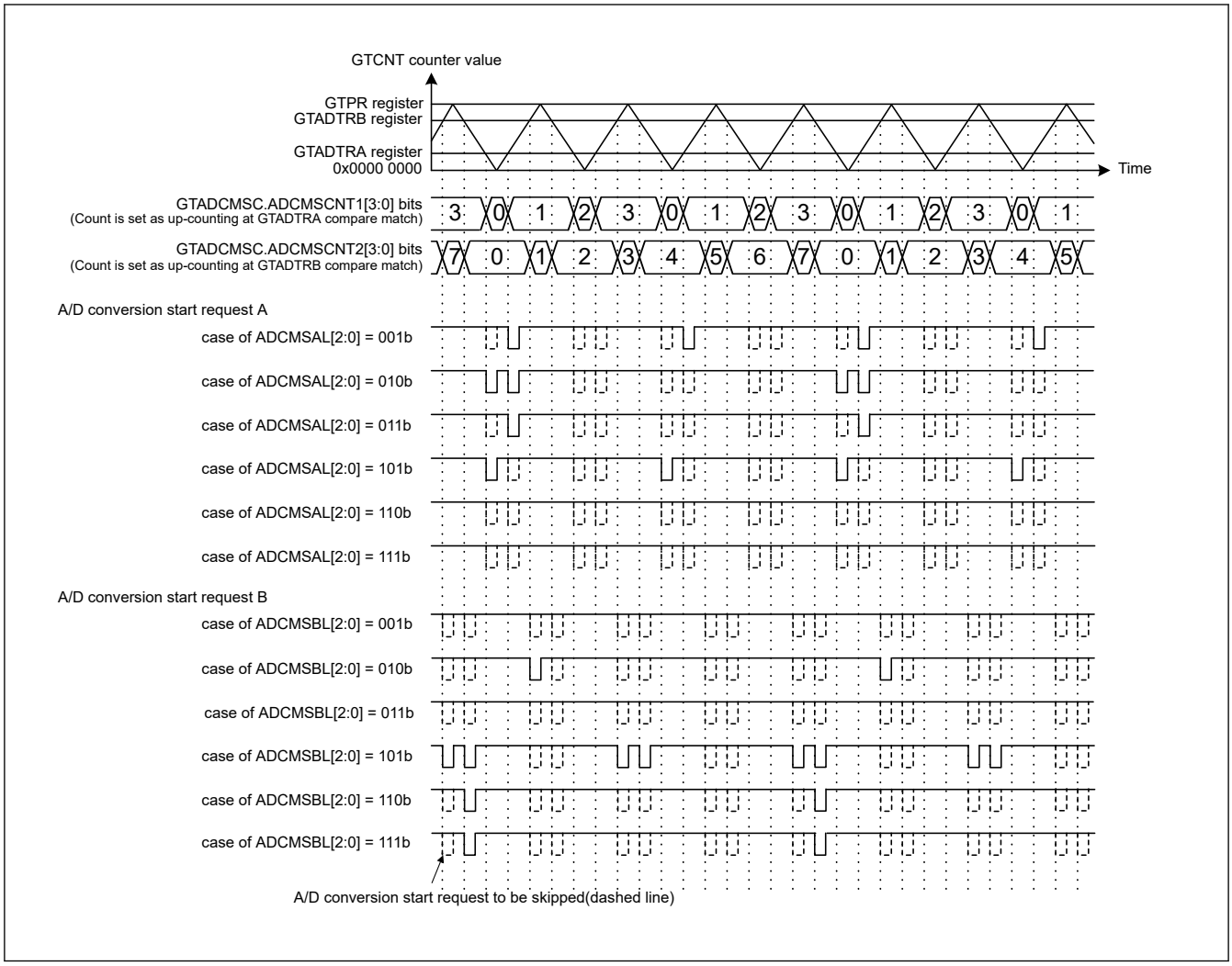


Figure 23.148 Example of A/D Conversion Start Request Compare Match Skipping Function Operation (Triangle wave, A/D Conversion Start Request Compare Match Skipping 1 Skipping Count: 3 Counting GTADTRA compare match, A/D Conversion Start Request Compare Match Skipping 2 Skipping Count: 7 Counting GTADTRB compare match)

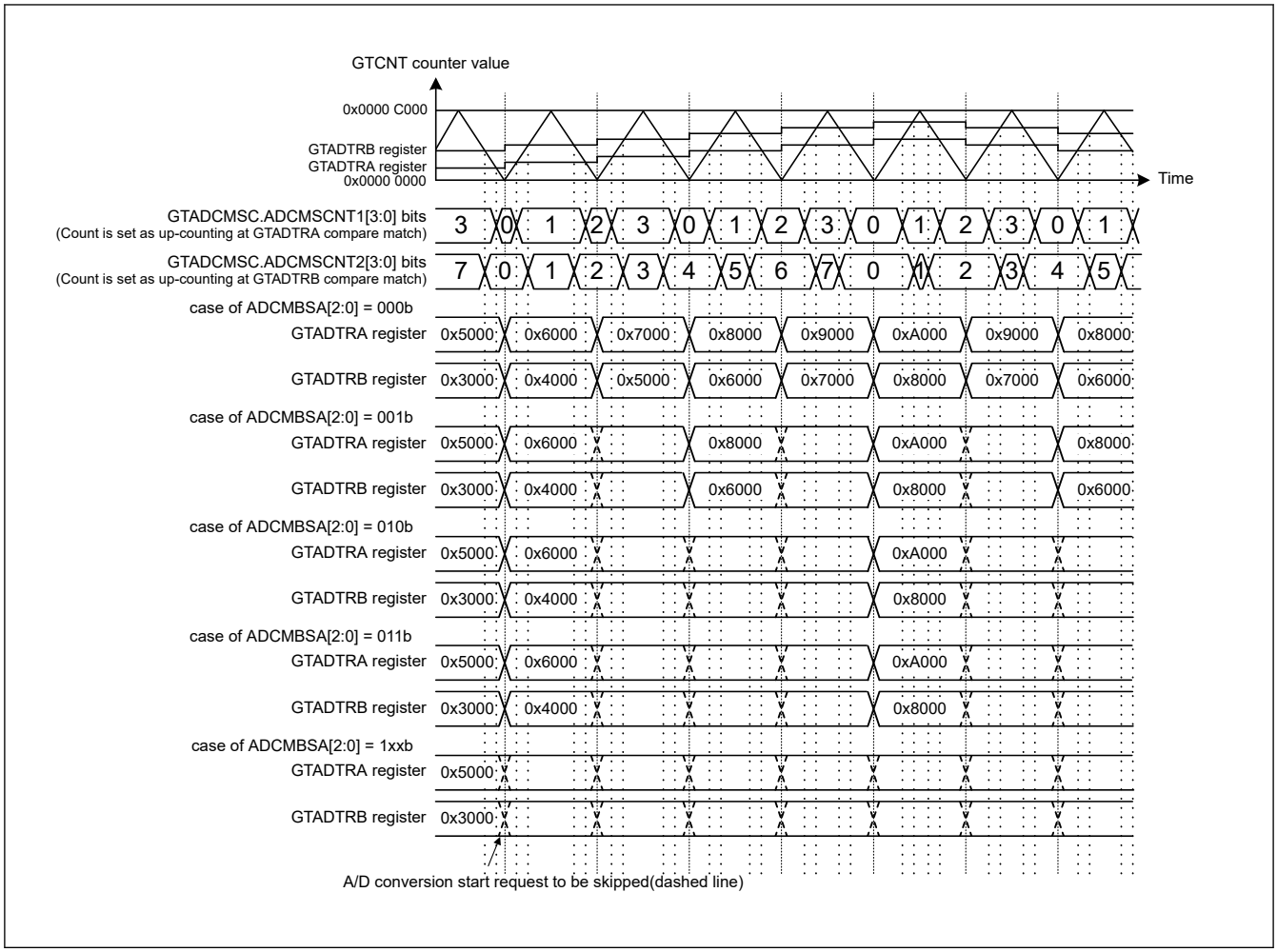


Figure 23.149 Example of A/D Conversion Start Request Compare Match Skipping Function Operation (Triangle wave, A/D Conversion Start Request Compare Match Skipping 1 Skipping Count: 3 Counting GTADTRA compare match, A/D Conversion Start Request Compare Match Skipping 2 Skipping Count: 7 Counting GTADTRB compare match, Buffer transfer of GTADTRA and GTADTRB at trough)

Table 23.73 shows an example of setting the A/D conversion start request compare match skipping.

The A/D conversion start request compare match skipping counter 2 initial value is set by the written value to the ADCMSCNT2IV[3:0] bits which is applied to change the setting from not counting the extended interrupt skipping counter 2 count source (GTADCMSC.ADCMSC2[1:0] bits = 00b) to counting (ADCMSC2[1:0] bits = other than 00b). Writing to the A/D conversion start request compare match skipping counter 2 initial value bit (ADCMSCNT2IV[3:0] bits) is performed only when the setting of the above-mentioned A/D conversion start request compare match skipping counter 2 initial value is written.

Table 23.73 Example for Setting the A/D Conversion Start Request Compare Match Skipping (1 of 2)

No.	Step Name	Description
1	Set GTCNT counter operation, Set buffer operation, Set compare match value	See section 23.3.2. Buffer Operation, section 23.3.3. PWM Output Operating Mode, section 23.5. A/D Conversion Start Request, and so on.
2	Set the A/D conversion start request compare match skipping function	Select the skipping counter and the skipping period with the skipping function select bit for the A/D conversion start request or the bit for the buffer transfer to be skipped in the GTADCMSS register.

Table 23.73 Example for Setting the A/D Conversion Start Request Compare Match Skipping (2 of 2)

No.	Step Name	Description
3	Set the A/D conversion start request compare match skipping counter k (k = 1, 2)	With the GTADCMSC register, set a count source of the skipping counter, skipping count, and the skipping counter k initial value as the following order. Set the GTADCMSC.ADCMSCk[1:0] bits as value other than 00b, and set the ADCMSTk[3:0] bits as value other than 0000b. Change the ADCMSCk[1:0] bits from 00b to value other than 00b as well as set the ADCMSCNTkIV[3:0] bits to the skipping counter k initial value.
4	Start count operation	Set GTCR.CST to 1 to start count operation.
5	Set buffer value for each cycle	See section 23.3.2. Buffer Operation, section 23.3.3. PWM Output Operating Mode, section 23.5. A/D Conversion Start Request, and so on.

23.5 A/D Conversion Start Request

The A/D conversion start request can be issued at a compare match between the GTCNT counter and the GTADTRA or GTADTRB register. Up-counting only, down-counting only, or both up-counting and down-counting can be specified by setting the GTINTAD register.

In complementary PWM mode, the A/D conversion start request can be issued at a compare match with the GTCNT counter of master channel.

During event count operation, the A/D conversion start request cannot be generated.

The A/D conversion start request is output directly to ADC16H.

The GTADTRA and GTADTRB registers each has two buffer registers. Buffer operation with the GTADTRA register used together with the GTADTBRA and GTADTDBRA registers, and buffer operation with the GTADTRB register used together with the GTADTBRB and GTADTDBRB registers can be performed.

The timing of the generation of requests to start A/D conversion can be monitored by an external pin. When the A/D conversion start request signal to be monitored is selected in the GTADSMR.ADSMSk bit (k = 0, 1) and when the output is enabled in the ADSMENk bit, a signal is output synchronized with a cycle frame of the timer used to generate the A/D conversion start request signal, of which the output is driven high at the generation of the A/D conversion start request signal by the GTADSMk pin, or at the end of the cycle of which the output is driven low. When a signal to request the start of A/D conversion is generated at the end of the cycle, the generation of this signal has priority in terms of monitoring output and the output remains at the high level till the end of the next cycle. The registers (GTADTRA and GTADTRB) that are sources of generating the A/D conversion start request signals and their counting directions can be checked by the A/D conversion start request flags (ADTRAUF, ADTRADF, ADTRBUF, and ADTRBDF) in the GTST register. When the output of the same A/D conversion start request signal monitoring output is enabled for multiple channels, ORed signals will be output from the GPT32.

Figure 23.150 shows an example of A/D conversion start request operation, Table 23.74 shows example for setting A/D conversion start request operation.

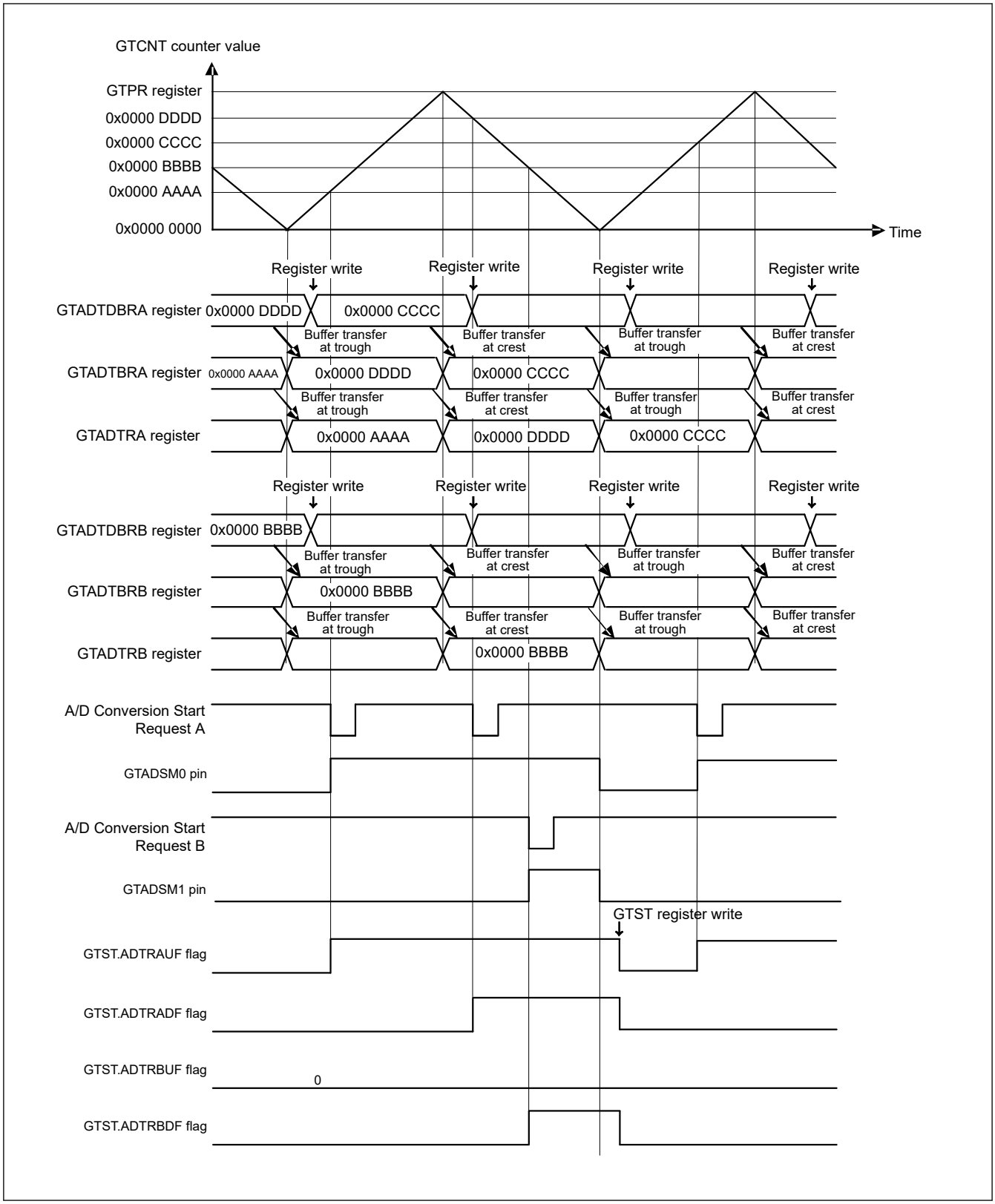


Figure 23.150 **Example of A/D Conversion Start Request Timing Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests, A/D Conversion Start Request by GTADTRA Register at Both Up-Counting and Down-Counting, A/D Conversion Start Request by GTADTRB Register at Down-Counting, Monitoring of the GTADTRA Register Up-Counting by the GTADSM0 Pin, Monitoring of the GTADTRB Register Down-Counting by the GTADSM1 Pin)**

Table 23.74 Example for Setting A/D Conversion Start Request Timing Operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 23.150, 100b, 101b, or 110b (0100b, 0101b, or 0110b) (triangle-wave PWM mode) is set.
2	Select count clock	Select the count clock with the GTCR.TPCS[3:0] bits.
3	Set cycle	Set the cycle in the GTPR register.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set buffer operation	Set buffer operation with the ADTTA[1:0], ADTTB[1:0], ADTDA, and ADTDB bits in the GTBER register. In Figure 23.150, ADTTA[1:0] = 11b, ADTTB[1:0] = 11b, ADTDA = 1, and ADTDB = 1.
6	Set compare match value	Set the A/D conversion start request point in the GTADTRA and GTADTRB registers.
7	Set buffer value	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.
8	Set A/D conversion start request for monitoring	Select the A/D conversion start request signal to be monitored with ADSMS0[1:0] and ADSMS1[1:0] bits in GTADSMR from GTADSM0 and GTADSM1 pins and enable output of the A/D conversion start request signal being monitored to ADSMEN0 and ADSMEN1 bits in GTADSMR. In Figure 23.150, ADSMS0[1:0] = 00b, ADSMS1[1:0] = 11b, ADSMEN0 = 1, and ADSMEN1 = 1.
9	Enable A/D conversion start request	Set to enable A/D conversion start request with the ADTRAUEN, ADTRADEN, ADTRBUEN, and ADTRBDEN bits in the GTINTAD register. In Figure 23.150, ADTRAUEN = 1, ADTRADEN = 1, ADTRBUEN = 0, and ADTRBDEN = 1.
10	Start count operation	Set the GTCR.CST bit to 1 to start count operation.
11	Set buffer value for each cycle	For buffer operation, set the A/D conversion start request point in one cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTBRA and GTADTBRB registers. For double buffer operation, also set the A/D conversion start request point in two cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or one cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in the GTADTDBRA and GTADTDBRB registers.

Figure 23.151 shows an example for A/D conversion start request timing operation.

This shows an example of the output of A/D conversion start request A as start source for the A/D converter. The A/D conversion start request A signal is output in response to a match in comparison with the GTADTRA register.

If GPT is operating with PCLKD and ADC is operating with PCLKA, A/D conversion start request A is passed to ADC on the next rising edge of PCLKA.

If GPT is operating with GPTCLK and ADC is also operating with GPTCLK, A/D conversion start request A is passed to ADC without delay.

For all other clock combinations, A/D conversion start request A is synchronized and passed to ADC.

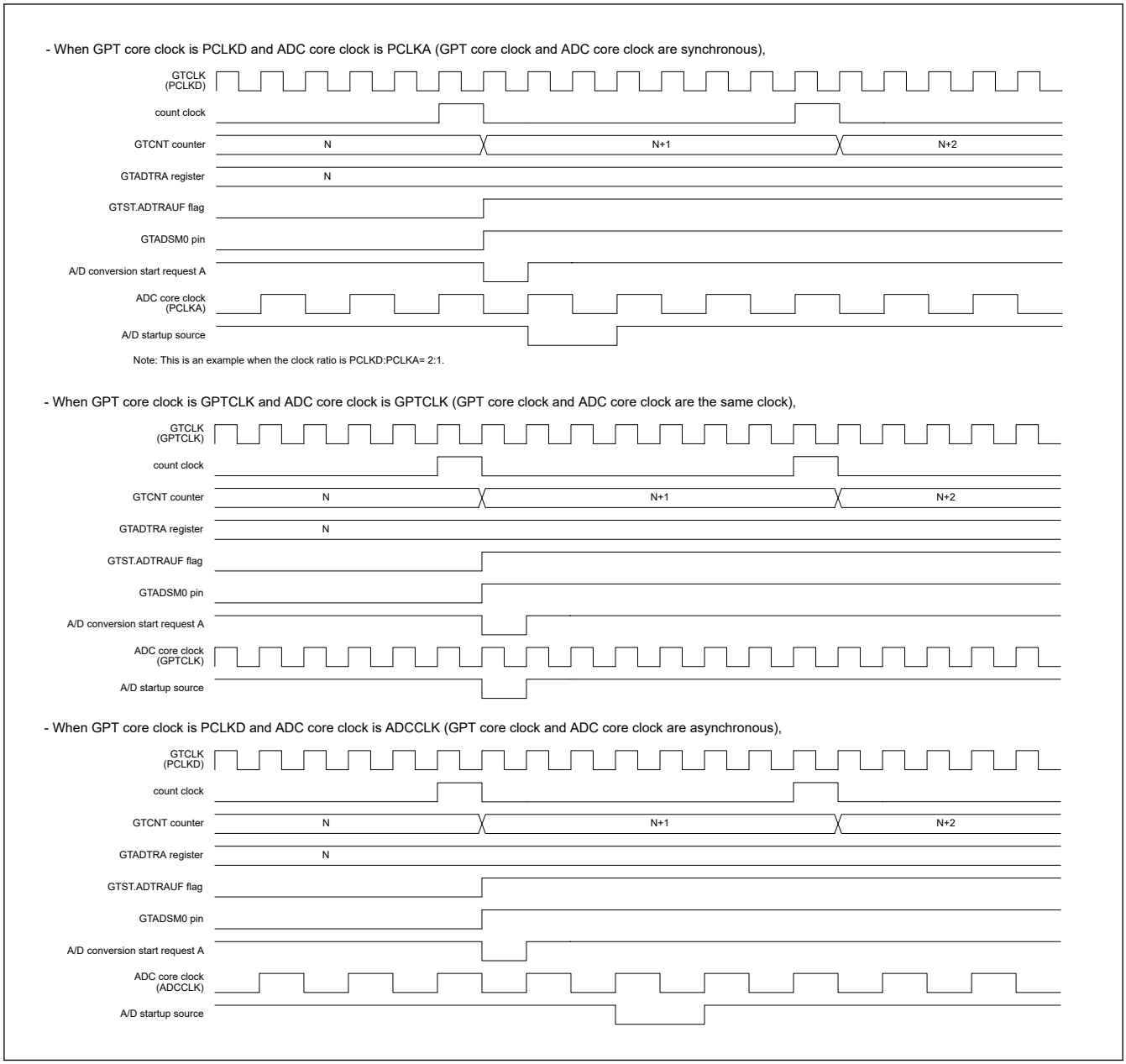


Figure 23.151 Example of A/D Conversion Start Request Timing Operation

For the restriction of A/D Conversion Start Request, see section 23.10.6. Interval of Interrupt Request.

23.6 Operations Linked by ELC

23.6.1 Event Signal Output to ELC

The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

The A/D conversion start request during up-counting/down-counting can be enabled/disabled individually with the A/D conversion start request enable bit to output events output to ELC.

The GPT has the following ELC event signals:

- Generation of compare match and input capture A interrupt (GPTn_CCMPA)
- Generation of compare match and input capture B interrupt (GPTn_CCMPB)
- Generation of compare match C interrupt (GPTn_CMPC)
- Generation of compare match D interrupt (GPTn_CMPD)

- Generation of compare match E interrupt (GPTn_CMPE)
- Generation of compare match F interrupt (GPTn_CMPF)
- Generation of overflow interrupt (GPTn_OVF)
- Generation of underflow interrupt (GPTn_UDF)
- Finish of period count function (GPTm_PC)

Note: n = 0 to 13
m = 0 to 3, 10 to 13

23.6.2 Event Signal Inputs from ELC

The GPT can perform the following operations in response to a maximum of 8 events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down-counting
- Input capture.

See section 20, Event Link Controller (ELC) for the connection between the ELC and the event signal input.

23.7 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than 3 sampling cycles.

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 23.152 shows the timing of noise filtering.

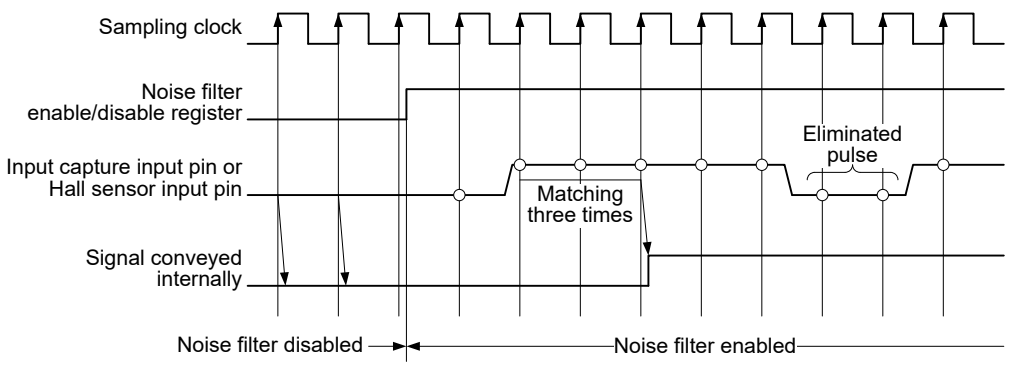


Figure 23.152 Timing of noise filtering

If noise filtering is enabled, the input capture operation or hall sensor input operation is performed on the edges of the noise filtered signal after a delay of (sampling interval × 2 + GTCLK) at the shortest. This is due to the noise filtering for the input capture input or hall sensor input.

23.8 Protection Function

23.8.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU,

GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR, GTADSMR, GTEITC, GTEITLI1, GTEITLI2, GTEITLB, GTICLF, GTPC, GTADCMSC, GTADCMSS, GTBER2, GTOLBR, GTICCR.

Every bit in registers GTSTR, GTSTP and GTCLR which can update the corresponding registers in other channels and can be updated by any of the corresponding registers in other channels conversely, can be protected by setting the GTWP.STRWP, STPWP, and CLRWP bits, respectively, per channel.

Likewise, writing to the GTSECSR and GTSECR registers, which can control all channels by writing to the GTSECSR and GTSECR registers of a given channel, can by enabled or disabled by the setting of the GTWP.CMNWP bit.

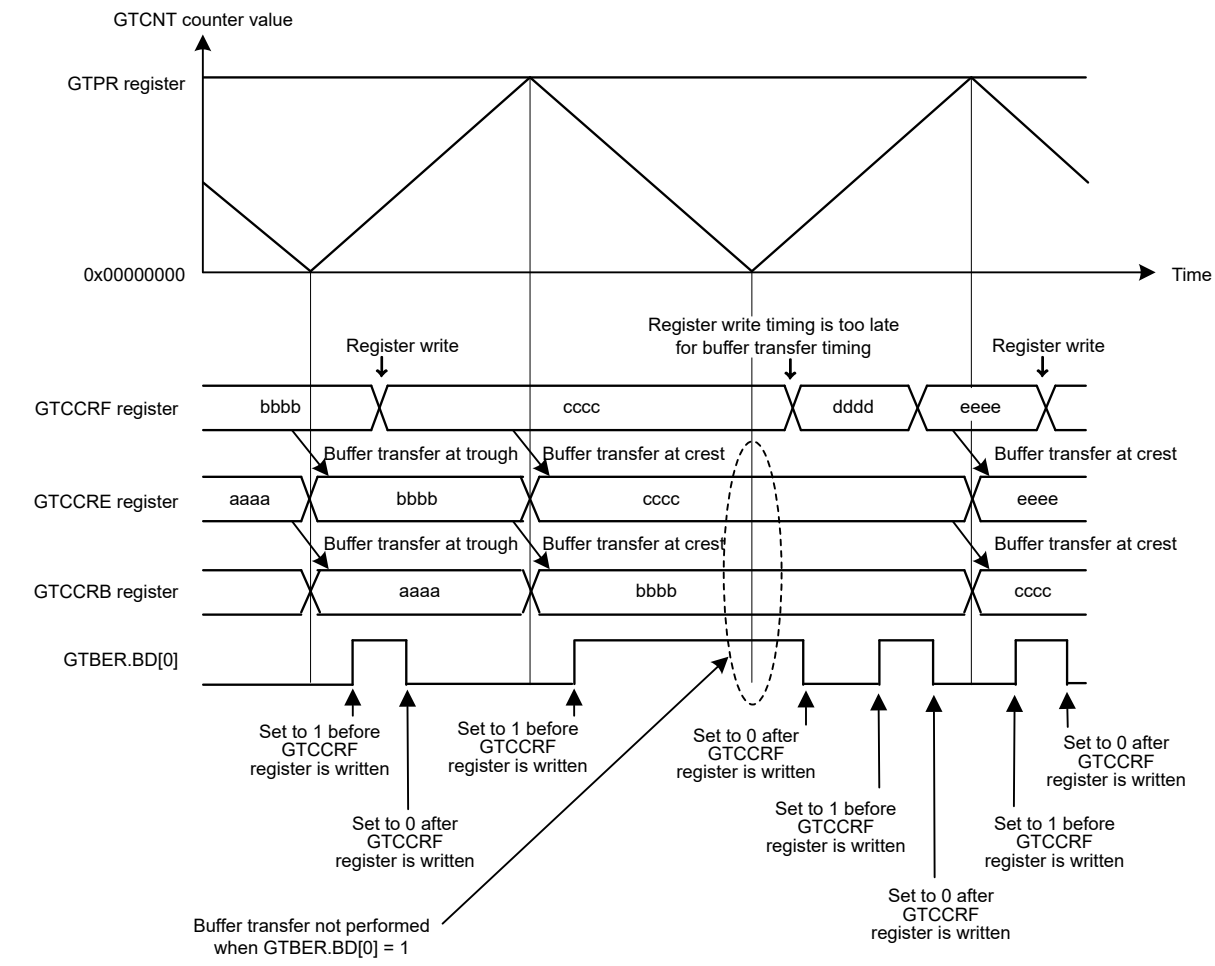
Protection using the GTWP register is only for write operations by the CPU. This protection does not cover updates to registers that occur in association with CPU writes.

23.8.2 Disabling of Buffer Operation

If the timing of the buffer register write is delayed relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD[3], BD[2], BD[1] and BD[0] bits settings. Specifically, buffer transfer can be temporarily disabled even though a buffer transfer condition is generated during buffer register write, by setting the BD[3], BD[2], BD[1] and BD[0] bits to 1 (buffer operation disabled) before buffer register write, and setting the bits to 0 (buffer operation enabled) after completion of writing to all the buffer registers.

The BD[3], BD[2], BD[1] and BD[0] bits can be set on channel basis by writing directly to the GTBER register or it can be set to 0 simultaneously by setting the GTSECR register for multiple channels which were set by the GTSECSR register.

Figure 23.153 shows an example of operation for disabling buffer operation by writing to the GTBER register.



Note: The base address of registers are the same.

Figure 23.153 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

23.8.2.1 Simultaneous Control of Buffer Operations of Multiple Channels

The GTBER.BD bit can be set by writing directly to the GTBER register per channel or by making settings in the GTSECR register for multiple channels that have already set in the GTSECSR register.

Follow the procedure below to simultaneously set the GTBER.BD bits of multiple channels.

1. Select the channels for simultaneously setting by the GTSECSR register
   Set the GTSECSR register so that the values at the bit positions for the corresponding channels for simultaneously setting of the GTBER.BD bits become 1. All GTSECSR registers can be updated by writing to the GTSECSR register of any channel.
2. Simultaneously set the GTBER.BD bits by updating the GTSECR register
   In the GTSECR register, set the operation of the GTBER.BD bits (enabling or disabling of buffer operation) which are to be simultaneously set. Writing to a GTSECR register from any channel updates the GTBER.BD bits in all channels corresponding to the bits set as 1 in the GTSECSR register, in accordance with the value of the GTSECR register.

Figure 23.154 and Figure 23.155 show examples of simultaneously controlling the enabling or disabling of buffer operation for multiple channels.

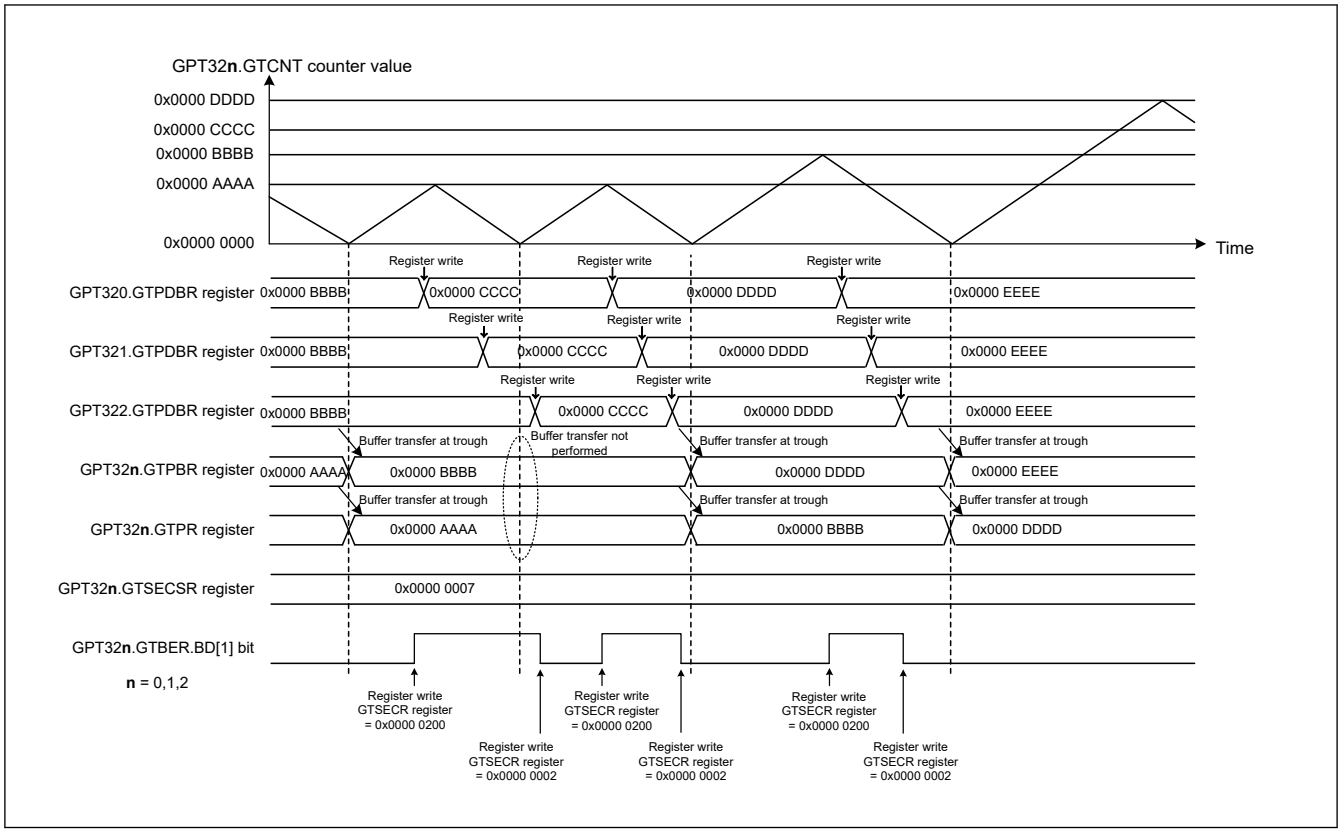


Figure 23.154 Example of Multiple Channel Operation for Disabling Buffer Operation (Triangle Waves, Double Buffer Operation)

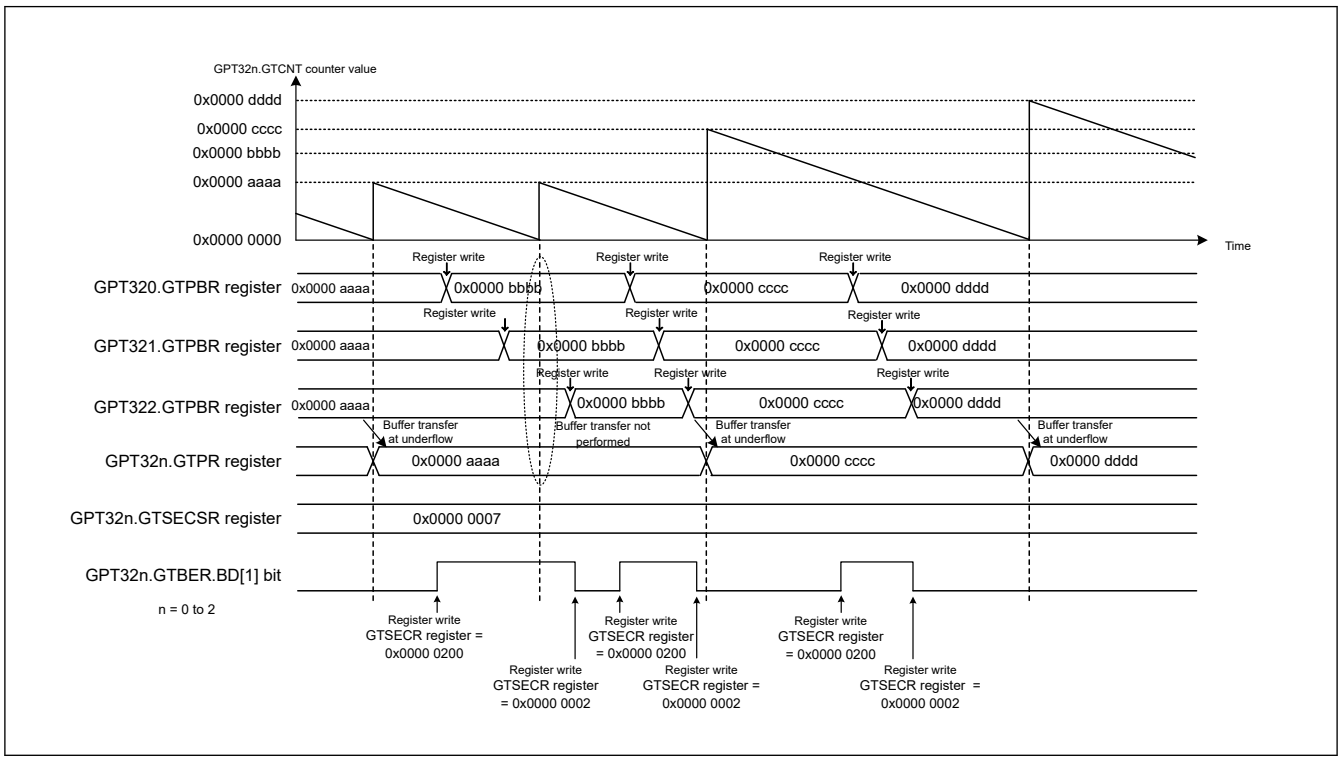


Figure 23.155 Example of Multiple Channel Operation for Disabling Buffer Operation (Saw Waves, Single Buffer Operation)

23.8.2.2 Repeated Double-Buffered Operation When Disabling GTCCR Buffer Transfer

When a GTBER.DBRTECm (m = A, B) bit is set to 1 in saw-wave one-shot pulse mode or triangle-wave PWM mode 3, transfer from the intermediate buffer to the GTCCRm (m = A, B) register is repeated on a cyclic basis even while buffer transfer is disabled by the setting of the GTBER.BD[0] bit or by the buffer transfer extended skipping function.

(1) In saw-wave one-shot pulse mode

In saw-wave one-shot pulse mode, the compare match value for the first half of a waveform is stored in temporary register x (x = C, E) as the intermediate buffer for the GTCCRx (x = C, E) register and the compare match value for the second half of a waveform is stored in temporary register m (m = A, B) as the intermediate buffer for the GTCCRy (y = D, F) register, respectively, for compare match values during repeated buffer operation, and the given values are alternately transferred to the GTCCRm (m = A, B) registers.

Table 23.75 lists the types of buffer transfer of the GTCCR register during counting in saw-wave one-shot pulse mode.

While counting is stopped, the setting of the value in the temporary register is transferred through forcible buffer transfer. In forcible buffer transfer, the values of the GTCCRy (y = D, F) registers are transferred to temporary registers m (m = A, B), and the values of the GTCCRx (x = C, E) are transferred to temporary registers x (x = C, E) when the setting of the corresponding GTBER.DBRTECm (m = A, B) bit is 1, respectively.

When the setting of the GTBER.DBRTECm (m = A, B) bit is 1, values written by the CPU to the GTCCRm (m = A, B) registers are reflected as the values of temporary registers x (x = C, E).

Table 23.75 GTCCR Buffer Transfer Operation in Saw-Wave One Shot Pulse Mode during GTCNT Counting

GTBER.DBRTECm	Buffer Transfer	Timing of transfer				
		GTCCRx ↓ GTCCRm	GTCCRx ↓ Temporary register x	Temporary register x ↓ GTCCRm	GTCCRy ↓ Temporary register m	Temporary register m ↓ GTCCRm
0	Transfer enabled period	Overflow or Underflow	No transfer	No transfer	Overflow or Underflow	GTCCRm compare match
	Transfer disabled period	No transfer	No transfer	No transfer	No transfer	No transfer
1	Transfer enabled period	Overflow or Underflow	Overflow or Underflow	No transfer	Overflow or Underflow	GTCCRm compare match
	Transfer disabled period	No transfer	No transfer	Overflow or Underflow	No transfer	GTCCRm compare match

Note: m = A, B
x = C, E
y = D, F

Figure 23.156 shows the operation of generating transfer-disabled period by extended buffer transfer skipping as an example of repeated double buffer operations when the GTCCR buffer transfer disabled in saw-wave one-shot pulse mode.

Figure 23.157 shows the operation of generating transfer-disabled period by updating the GTBER.BD[0] bit as an example of repeated double-buffer operations when the GTCCR buffer transfer is disabled in saw-wave one-shot pulse mode.

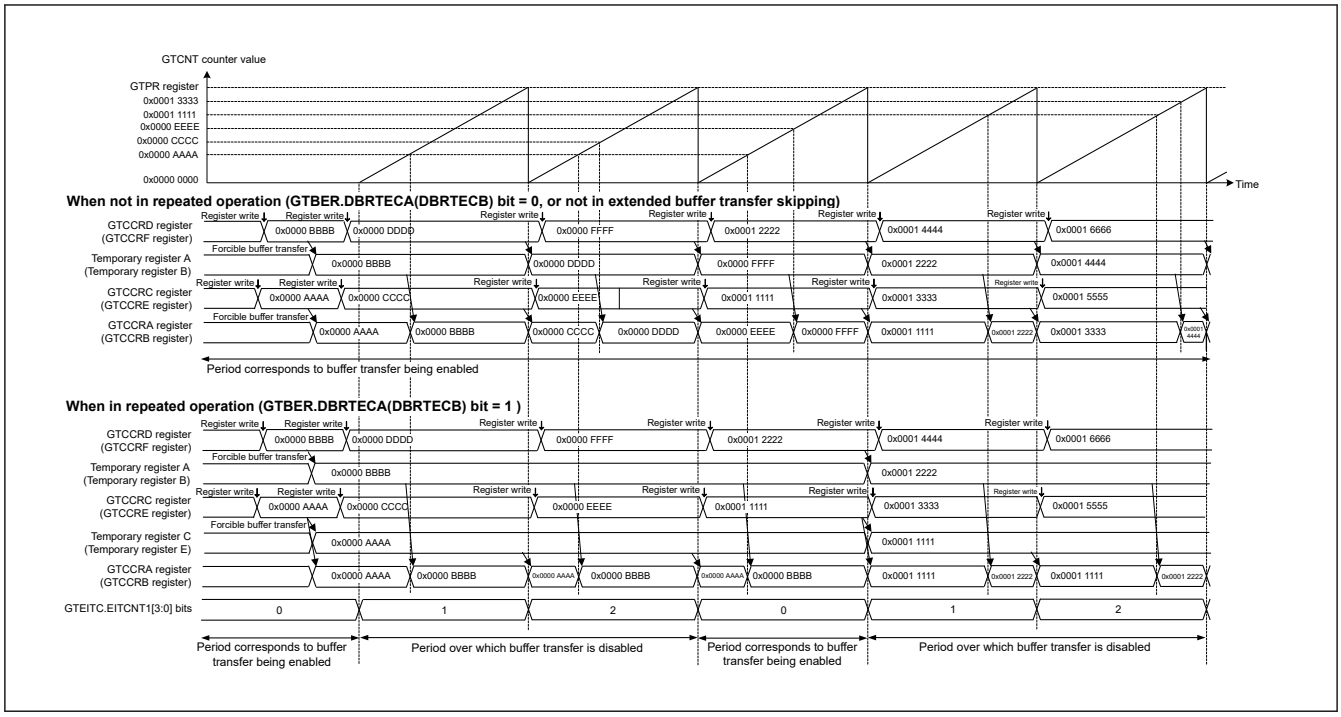


Figure 23.156 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Saw-Wave One-Shot Pulse Mode, Using Extended Buffer Transfer Skipping, GTBER.BD[0] is Constantly 0)

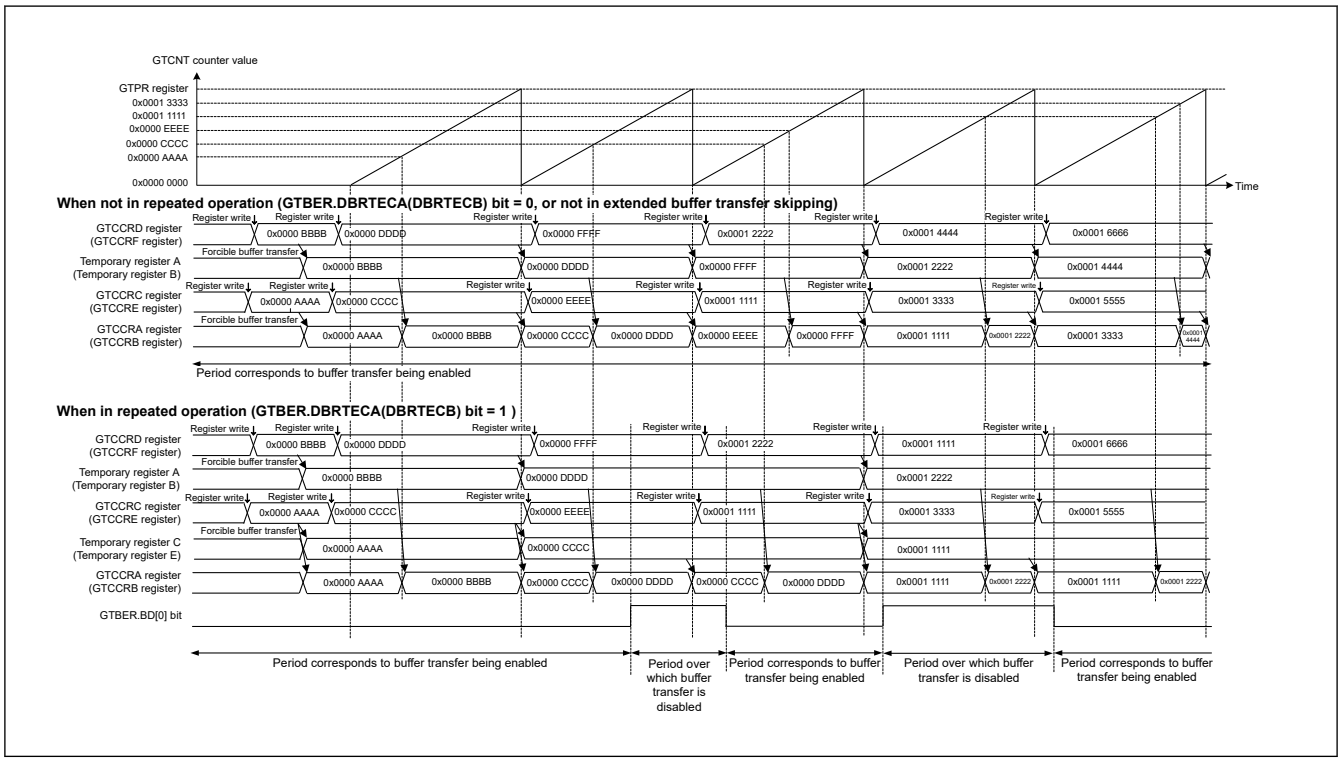


Figure 23.157 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Saw-Wave One-Shot Pulse Mode, Updating the GTBER.BD[0] Bit)

(2) In triangle-wave PWM mode 3

In triangle-wave PWM mode 3, the compare match value for the first half of a waveform is stored in the temporary register x (x = C, E) as the intermediate buffer for the GTCCRx (x = C, E) register and the compare match value for the second half of a waveform is stored in temporary register m (m = A, B) as the intermediate buffer for the GTCCRy (y = D, F) register,

respectively, for compare match values during repeated buffer operation, and the given values are alternately transferred to the GTCCRm (m = A, B) register.

Table 23.76 lists the types of buffer transfer of the GTCCR register during counting operation in triangle-wave PWM mode 3.

While counting is stopped, the setting of the value in the temporary register is transferred through forcible buffer transfer. In forcible buffer transfer, the values of the GTCCRy (y = D, F) registers are transferred to temporary registers m (m = A, B), and the values of the GTCCRx (x = C, E) are transferred to temporary registers x (x = C, E), when the setting of the corresponding GTBER.DBRTECm (m = A, B) bit is 1, respectively.

When the setting of the GTBER.DBRTECm (m = A, B) bit is set to 1, values written by the CPU to the GTCCRm (m = A, B) registers are reflected as the values of temporary registers x (x = C, E).

Table 23.76 GTCCR Buffer Transfer Operation in Triangle-Wave PWM Mode 3 during GTCNT Counting

GTBER.DBRTECm	Buffer Transfer	Timing of transfer				
		GTCCRx ↓ GTCCRm	GTCCRx ↓ Temporary register x	Temporary register x ↓ GTCCRm	GTCCRy ↓ Temporary register m	Temporary register m ↓ GTCCRm
0	Transfer enabled period	Trough	No transfer	No transfer	Trough	Crest
	Transfer disabled period	No transfer	No transfer	No transfer	No transfer	No transfer
1	Transfer enabled period	Trough	Trough	No transfer	Trough	Crest
	Transfer disabled period	No transfer	No transfer	Trough	No transfer	Crest

Note: m = A, B
x = C, E
y = D, F

Figure 23.158 shows the operation of generating transfer-disabled period by extended buffer transfer skipping as an example of repeated double buffer operations when the GTCCR buffer transfer disabled in triangle-wave PWM mode 3.

Figure 23.159 shows the operation of generating transfer-disabled period by updating the GTBER.BD[0] bit as an example of repeated double-buffer operations when the GTCCR buffer transfer is disabled in triangle-wave PWM mode 3.

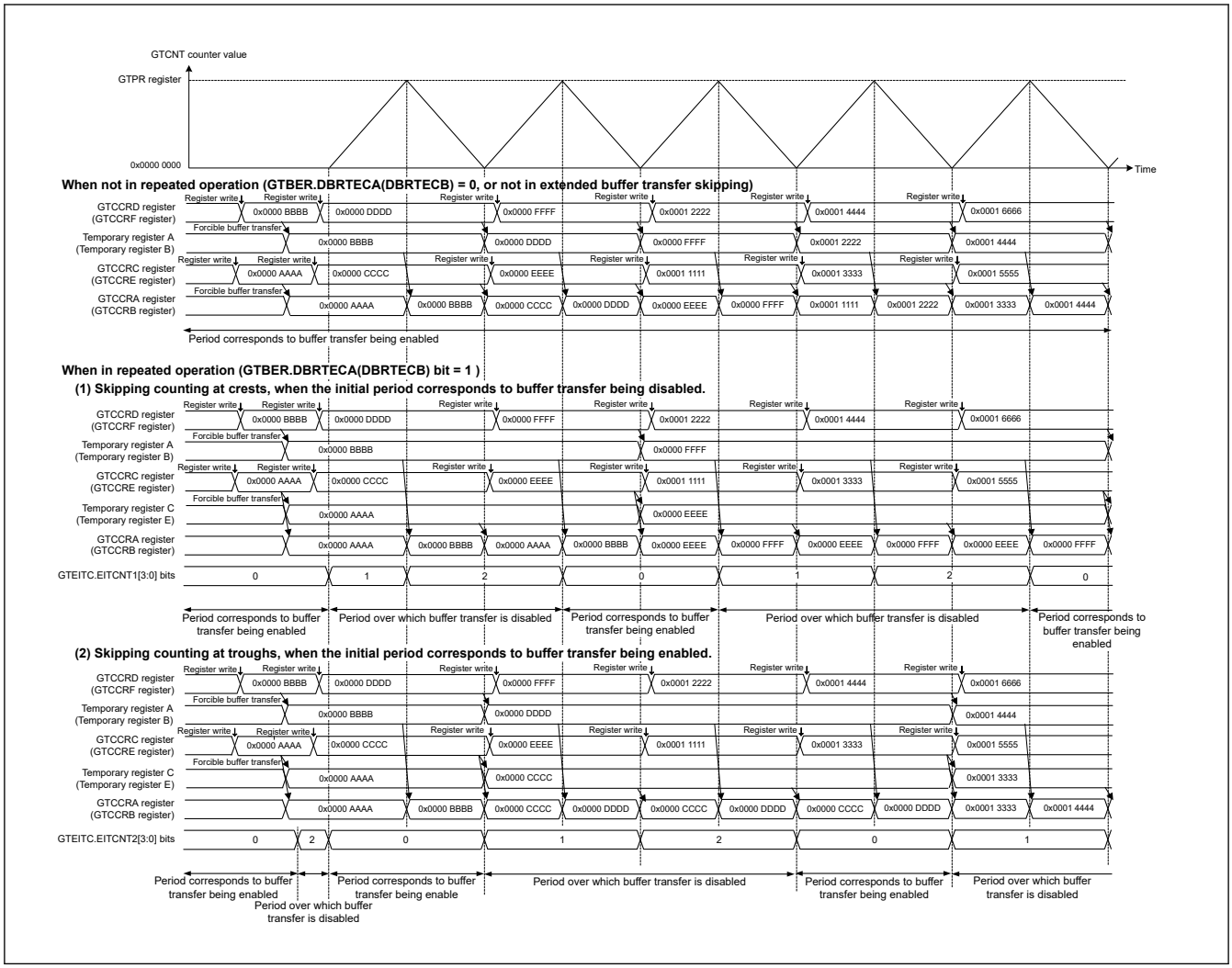


Figure 23.158 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Triangle-Wave PWM Mode 3, Using Extended Buffer Transfer Skipping, GTBER.BD[0] is Constantly 0)

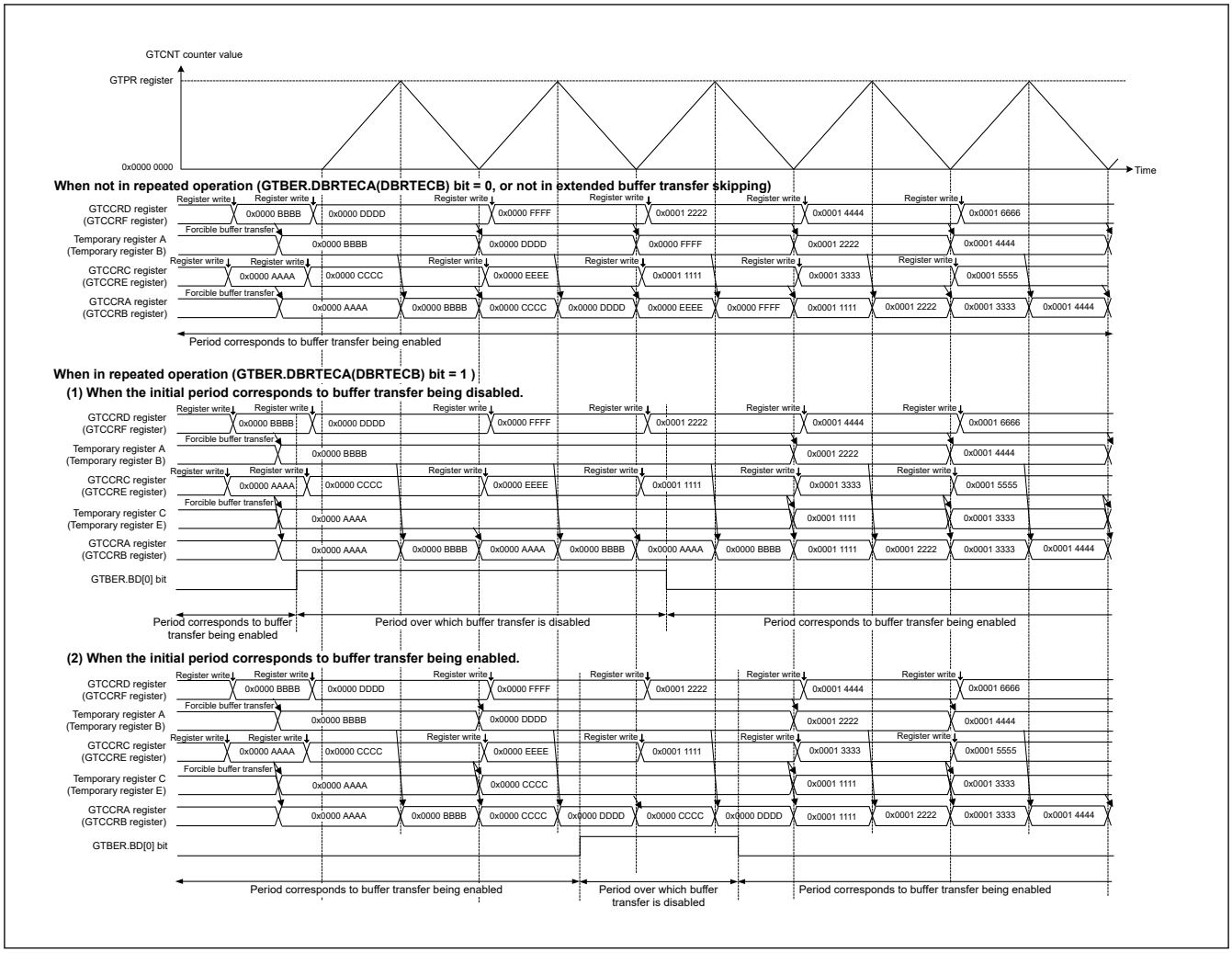


Figure 23.159 Example of Repeated Double-Buffer Operation When GTCCR Buffer Transfer is Disabled (Triangle-Wave PWM Mode 3, Updating the GTBER.BD[0] Bit)

23.8.3 GTIOCnm Pin Output Negate Control (n = 0 to 13, m = A, B)

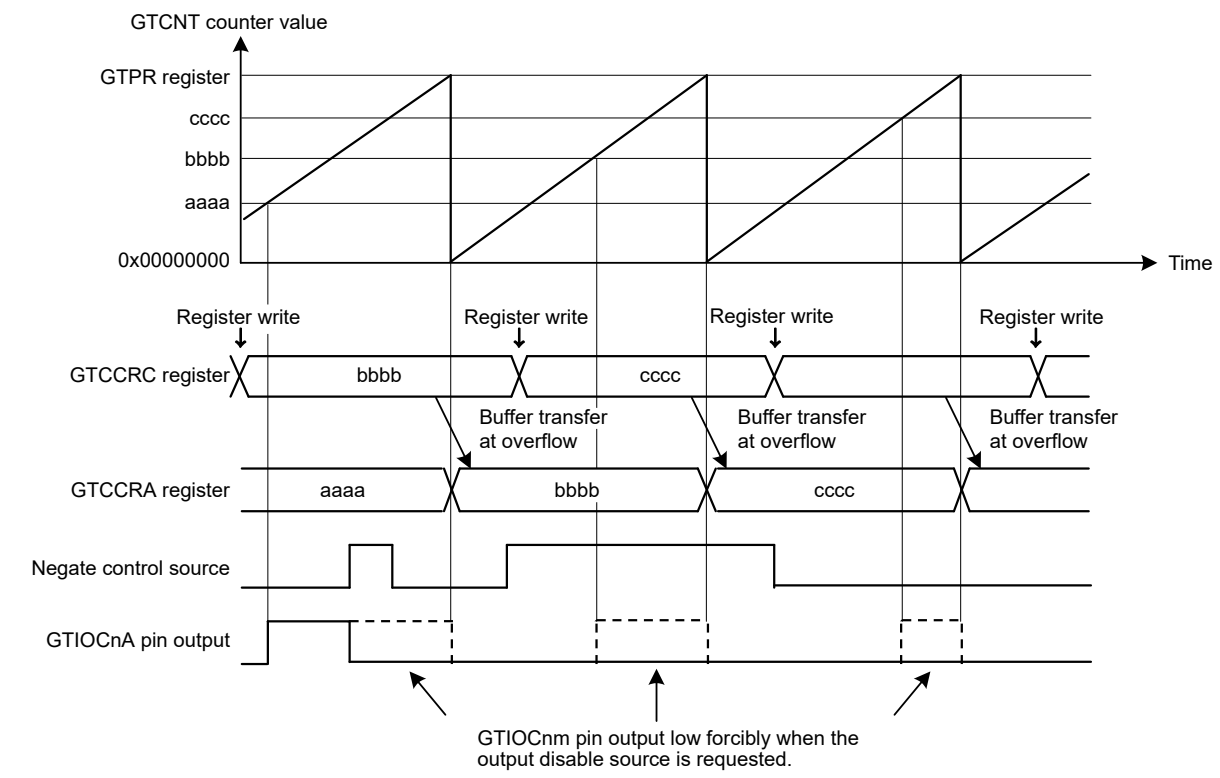
For protection from system failure, the output disable control that changes the GTIOCnm pin output value forcibly is provided for GTIOCnm pin output by the request of output disable from POEG. Output protection is required when a dead time error or the same output level being on the GTIOCnA and GTIOCnB pins is detected. GPT detects this condition and generates output disable requests to POEG according to the setting of the output disable request permission bits, such as GTINTAD.GRPDTE, GTINTAD.GRPABH, GTINTAD.GRPABL. After the POEG performs the logical OR of the output disable request from each channel and the output disable request from the external input, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCnA pin and the GTIOCnB pin) out of 4 output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is set based on the GTIOR.OADF[1:0] bits for the GTIOCnA pin and the GTIOR.OBDF[1:0] setting for the GTIOCnB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request. It is after 3 GTCLK at shortest when the output disable condition is released after the output disable request becomes no longer satisfied. To reliably control output disabling, clear the flag of POEG for which the condition for the request to disable the output is no longer satisfied after 4 cycles of GTCLK.

When event count is performed or when the operating mode is saw-wave PWM mode 2 or when the output disable state should be released immediately without waiting for end of cycle, GTIOR.OADF[1:0] should be set to 00b (for GTIOCnA pin) or GTIOR.OBDF[1:0] should be set to 00b (for the GTIOCnB pin).

Figure 23.160 shows an example of the GTIOCnm pin output disable control operation. (n = 0 to 13, m = A, B)



Note: The base address of registers are the same.

Figure 23.160 Example of GTIOCnm pin output disable control operation in saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable (n = 0 to 13, m = A, B)

23.8.4 Output Protection Function for GTIOCnm Pin Output (n = 0 to 13; m = A, B)

To prepare for a case when an incorrect value (0x0000 0000 or a value greater than or equal to the GTPR register value) is set in the GTCCRA register, the output protection function for the GTIOCnm pin output (disabling function) is activated when the automatic dead time is set (GTDTCR.TDE bit = 1) in triangle-wave PWM mode.

The status of the output protection function can be read from the GTSOS.SOS[1:0] bits.

Figure 23.161 shows the output protection function state transition.

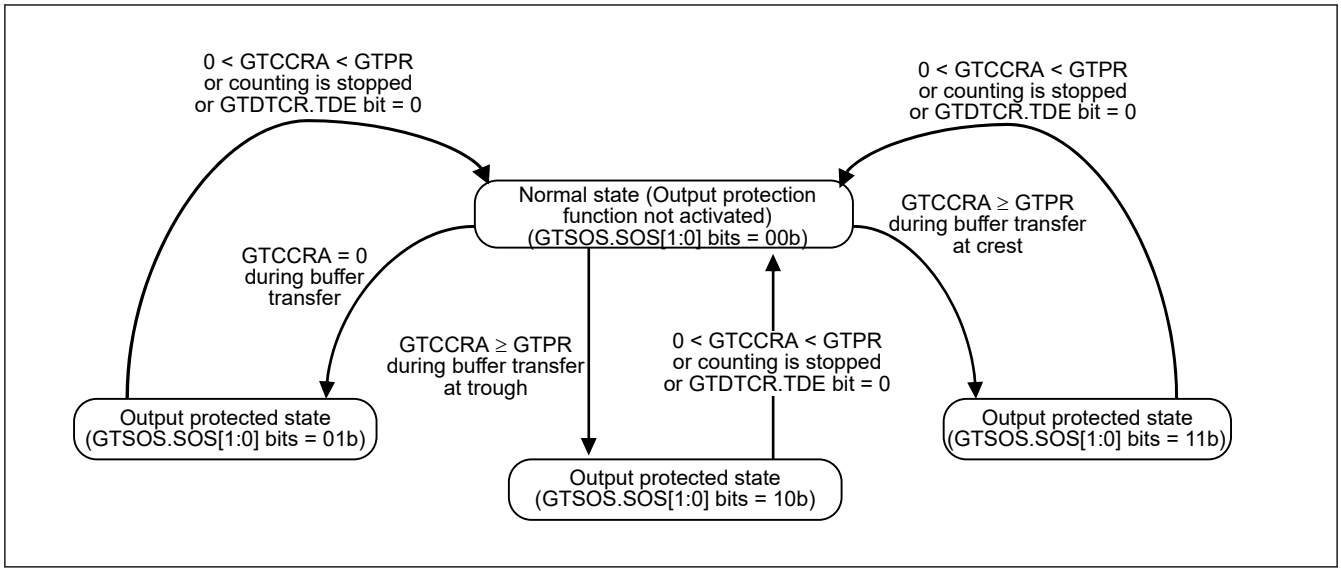


Figure 23.161 Output Protection Function

(1) Output Protection Function When the GTCCRA Register is Set to 0x0000 0000 during Buffer Transfer

Figure 23.162 and Figure 23.163 show examples of output protection function operation when the GTCCRA register is set to 0x0000 0000 during buffer transfer at troughs, and Figure 23.164 and Figure 23.165 show examples when the GTCCRA register is set to 0x0000 0000 during buffer transfer at crests.

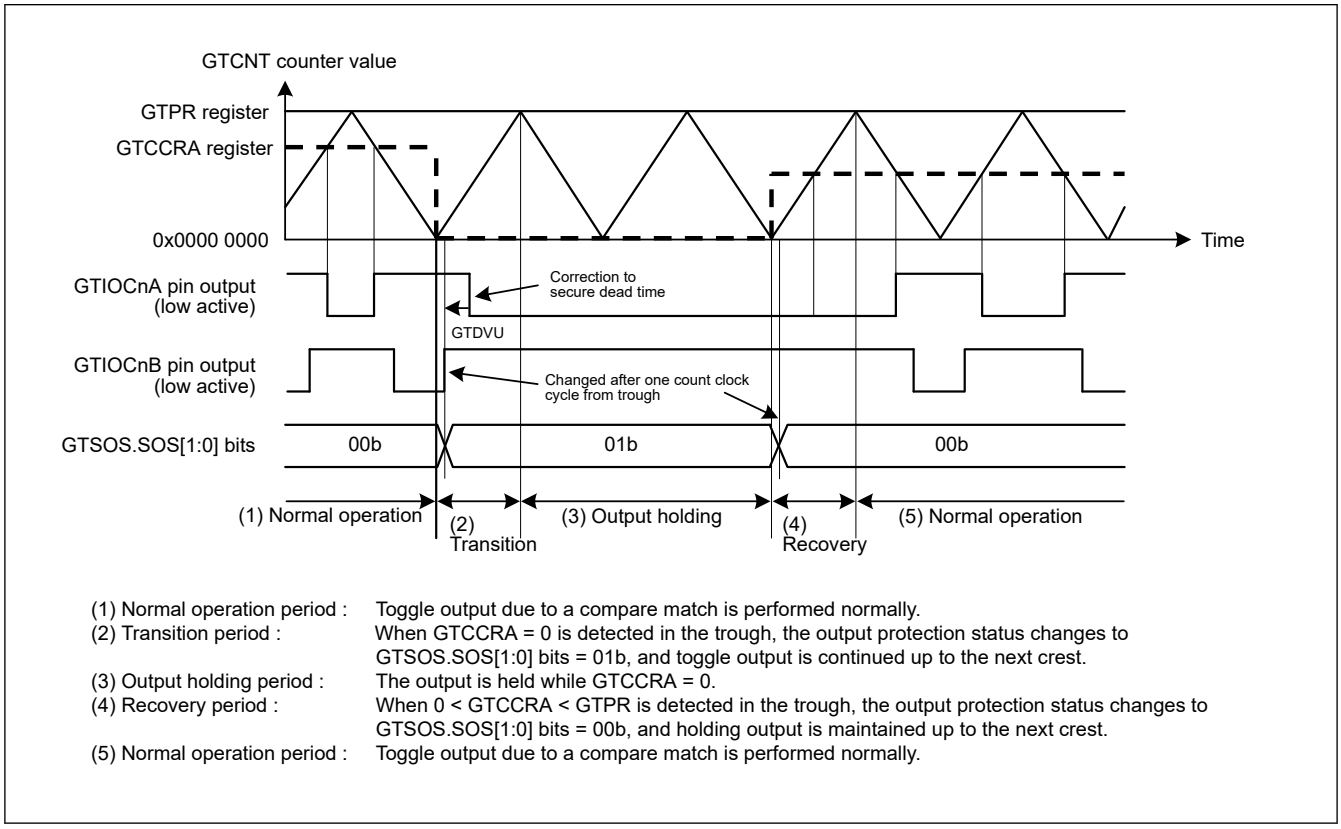
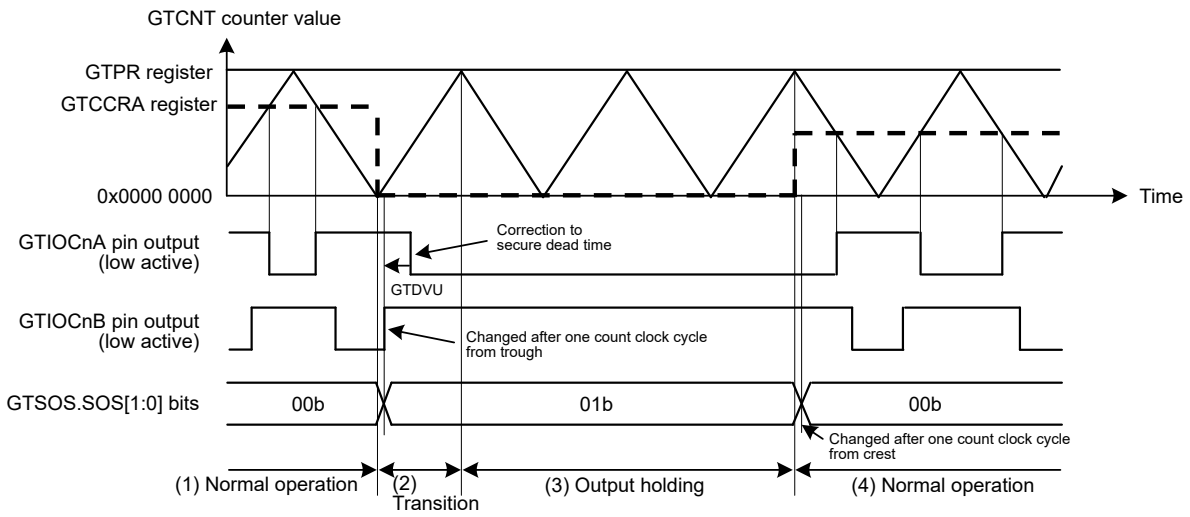
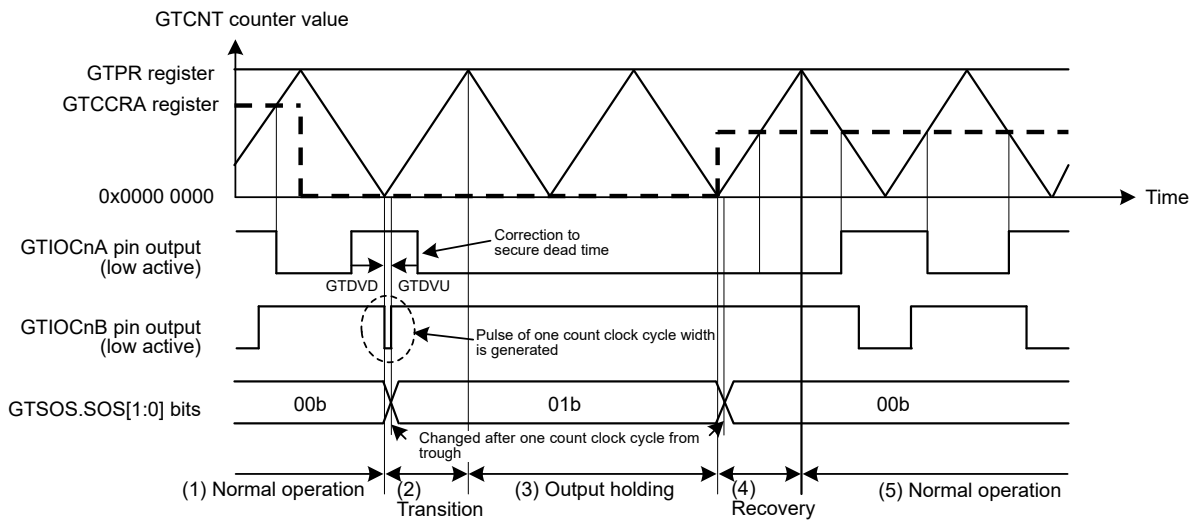


Figure 23.162 Example of Output Protection Function Operation When GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 13)



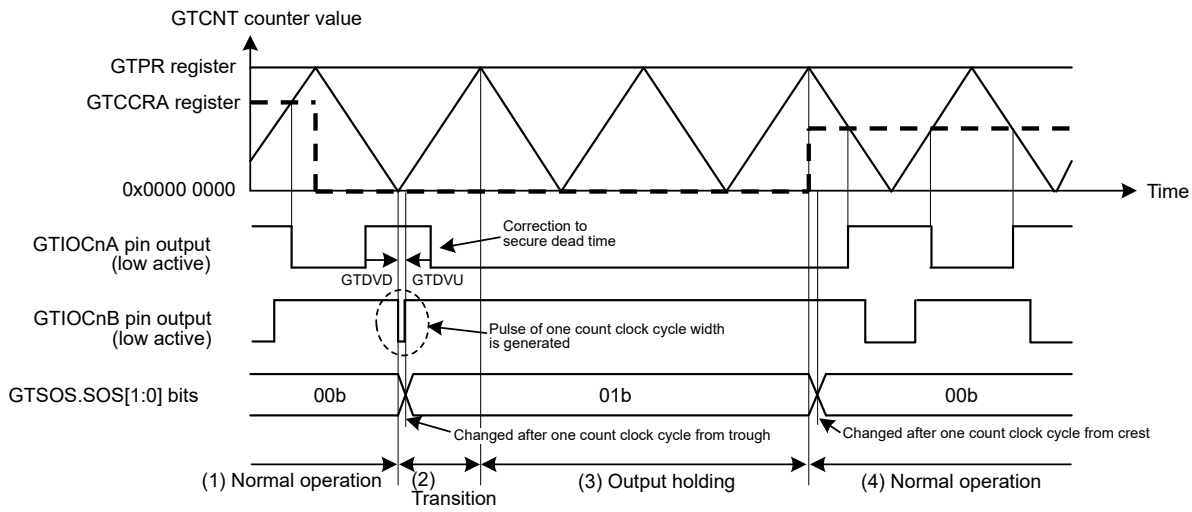
(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Transition period : When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period : The output is held while GTCCRA = 0.
(4) Normal operation period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.163 Example of Output Protection Function Operation When GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 13)



(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Transition period : When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding : The output is held while GTCCRA = 0.
(4) Recovery period : When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period : Toggle output due to a compare match is performed normally.

Figure 23.164 Example of Output Protection Function Operation When GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 13)

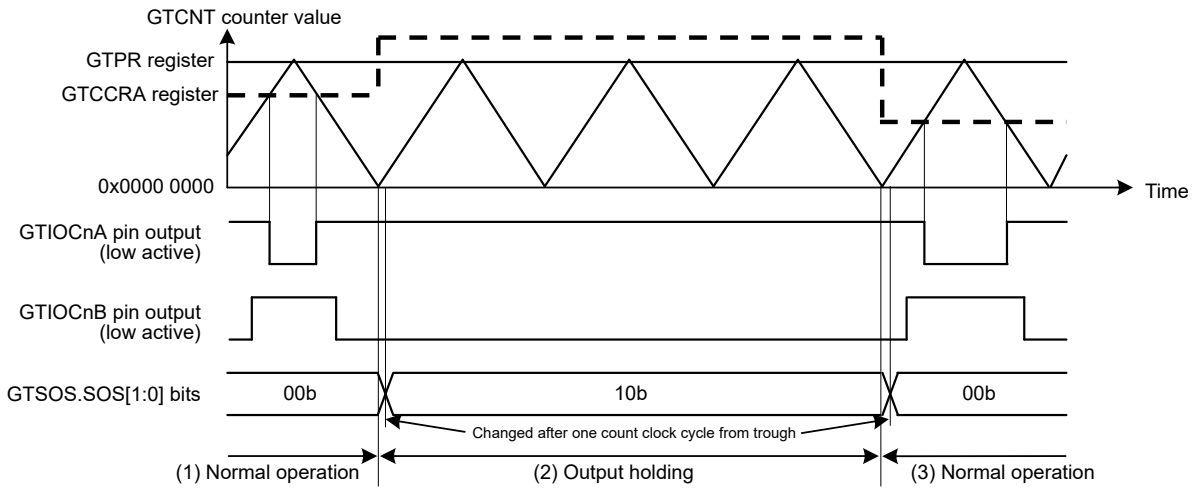


(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Transition period : When GTCCRA = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period : The output is held while GTCCRA = 0.
(4) Normal operation period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.165 Example of Output Protection Function Operation When the GTCCRA is Set to 0x0000 0000 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 13)

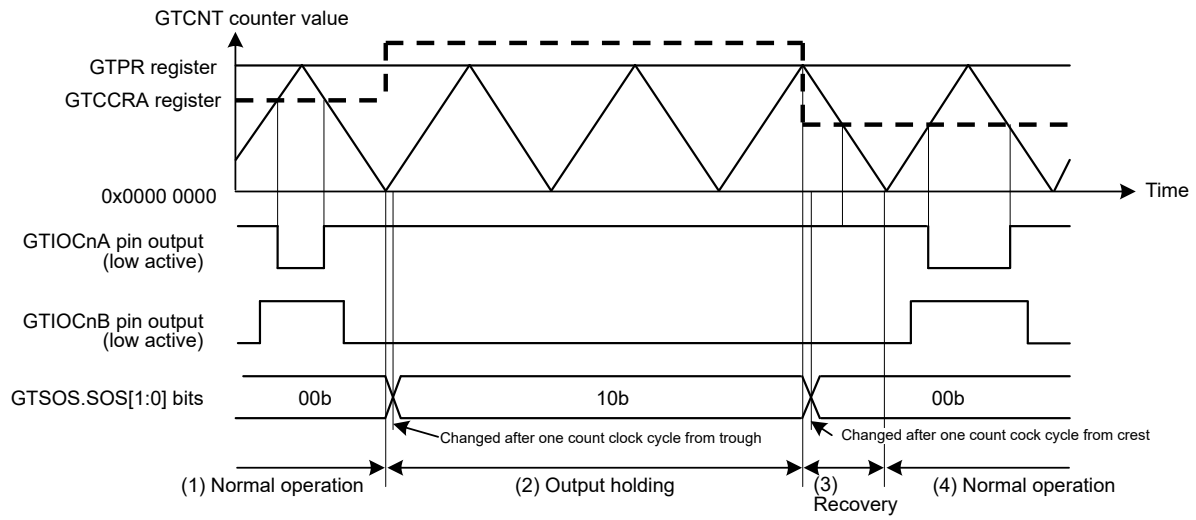
(2) Output Protection Function When GTCCRA Register ≥ GTPR Register is Set during Buffer Transfer at Troughs

Figure 23.166 and Figure 23.167 show examples of output protection function operation when GTCCRA register ≥ GTPR register is set during buffer transfer at troughs.



(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period : When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.166 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 13)

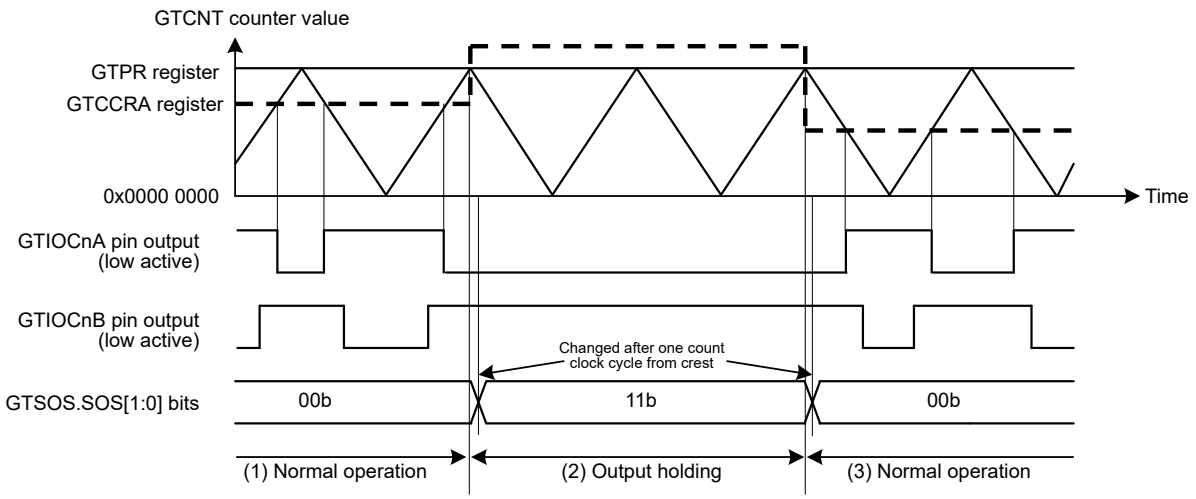


(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period : Toggle output due to a compare match is performed normally.

Figure 23.167 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 13)

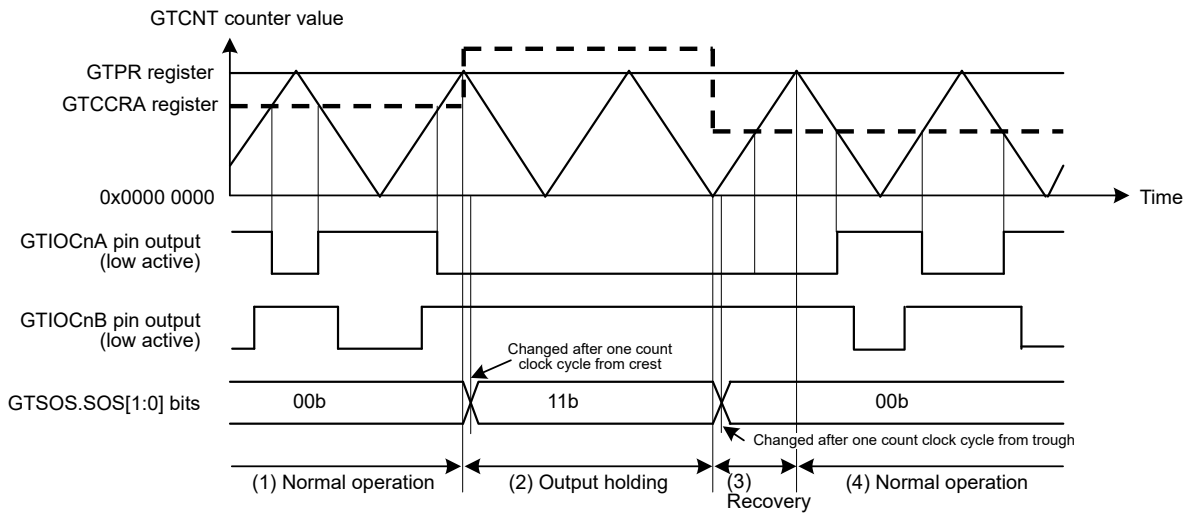
(3) Output Protection Function When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests

Figure 23.168 and Figure 23.169 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests.



(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period : When 0 < GTCCRA < GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.168 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low) (n = 0 to 13)



(1) Normal operation period : Toggle output due to a compare match is performed normally.
(2) Output holding period : When GTCCRA ≥ GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period : When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(4) Normal operation period : Toggle output due to a compare match is performed normally.

Figure 23.169 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 13)

(4) Restricted Specification of Output Protection Function

Even if an incorrect value (0x0000 0000 or a value greater than or equal to the GTPR register value) is set in the GTCCRA register during count operation, the output protection functions in a specific way such that one of the positive- and negative-phase outputs becomes non-active. However, if the following condition is not satisfied, the output protection does not operate normally.

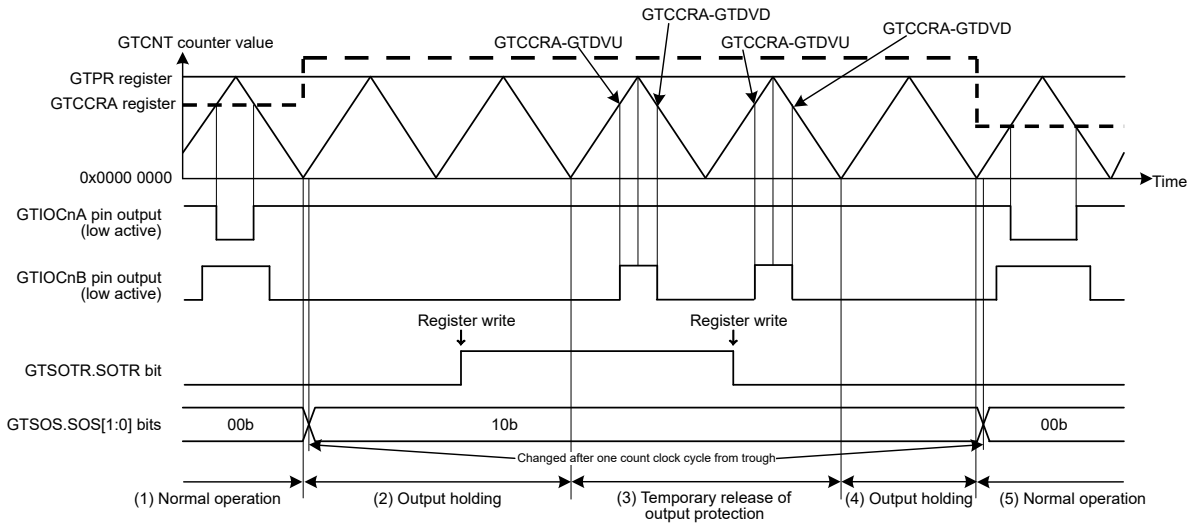
- When the GTCCRA register value at the start of count operation is greater than 0x0000 0000, and less than the setting value of the GTPR register

(5) Temporary Release of Output Protection Function

When the GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA register ≥ GTPR register has occurred during transfer at trough), the protected state of the GTIOCnB pin output can be temporarily released by setting the GTSOTR.SOTR bit to 1. The SOS[1:0] bits retain 10b even if the output protection function is released.

When the SOTR bit is set to 0, the GTIOCnB pin output protection can be restarted.

Figure 23.170 shows examples of the operation of temporary release of output protection when the setting of the GTCCRA register ≥ GTPR register during buffer transfer at troughs.



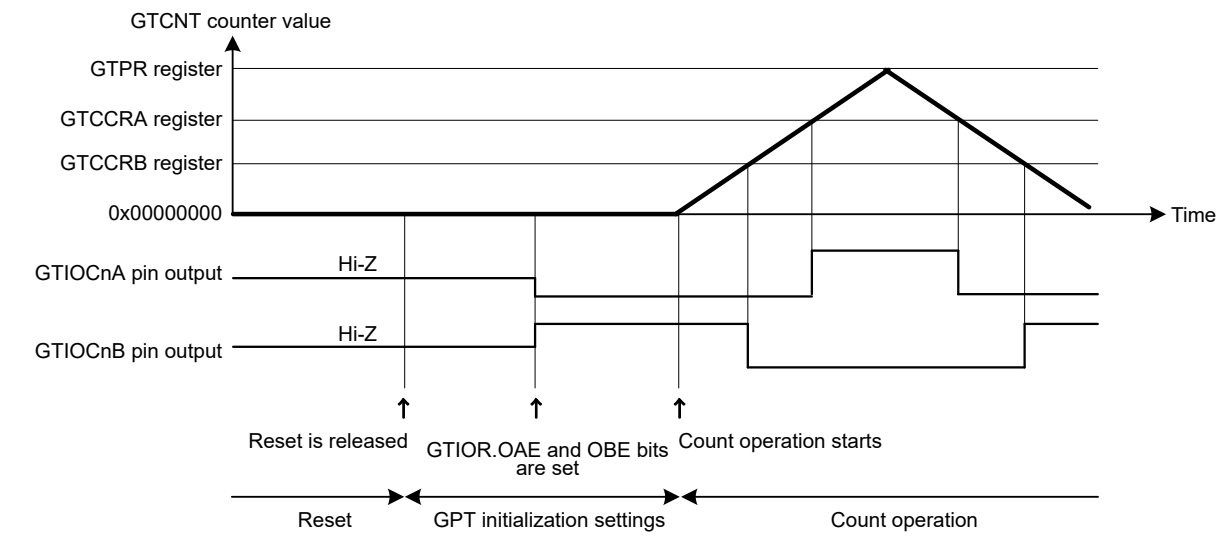
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA ≥ GTPR.
Even when the GTSOTR.SOTR bit is set to 1 during the output holding period, the GTIOCnB pin output is held until the first trough after the setting.
(3) Output protection temporary release period: After GTSOTR.SOTR bit is set to 1, the GTIOCnB pin output is performed normally from the first trough after the setting.
Even when the GTSOTR.SOTR bit is set to 0 during the output protection releasing period, the GTIOCnB pin output is held until the first trough after the setting.
(4) Output holding period: The output is held until 0 < GTCCRA < GTPR is detected in the trough.
(5) Normal operation period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.170 Example of Temporary Release of Output Protection When the Setting of the GTCCRA ≥ GTPR during Buffer Transfer at Trough s (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low) (n = 0 to 13)

23.9 Initialization Method of Output Pins

23.9.1 Pin Settings After Reset

The GPT registers are initialized at a reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial low output, output retained at cycle end, output toggled at compare match
GTIOR.GTIOB[4:0] bits: Initial high output, output retained at cycle end, output toggled at compare match

Note: The base address of registers are the same.

Figure 23.171 Example of pin settings after reset

23.9.2 Pin Initialization Due to Error During Operation

If an error occurs during GPT operation, the following four types of pin control can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR registers and PmnPFS.PMR bit of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0, and the control bit associated with the pin in the PMR to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

If the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting is resumed, operation continues from where it stopped. If counting is stopped, the registers must be initialized before counting starts.

23.10 Usage Notes

23.10.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Mode.

Set GTCLKCR register before releasing the module-stop state.

23.10.2 GTCCRn Settings During Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy all of the following conditions:

- GTDVU < GTCCRA
- GTCCRA > GTDVD

- 0 < GTCCRA < GTPR

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made for the GTCCRA register during count operation, the output protection function is activated. However, if the following condition is not satisfied, the output protection function does not work normally:

- The value of the GTCCRA register at the start of counting is larger than 0 and less than GTPR.

For details, see section 23.8.4. Output Protection Function for GTIOCnm Pin Output (n = 0 to 13; m = A, B)

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB is 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVD

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

(6) In Complementary PWM mode 1, 2, 3

The GTCCRn register must be set with the range of 0 ≤ GTCCRn ≤ GTPR + GTDVU.

(7) In Complementary PWM mode 4

In single buffer operation, the GTCCRn register must be set with the range of 0 ≤ GTCCRn ≤ GTPR + GTDVU.

In double buffer operation, the GTCCRn register must be set with the range of GTDVU < GTCCRn < GTPR.

23.10.3 Setting Range for GTCNT Counter

Other than the Saw-wave PWM mode 2 and Complementary PWM mode, the GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

23.10.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[3:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[3:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in situations in which an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

23.10.5 Priority Order of Each Event

(1) GTCNT register

Table 23.77 shows a priority order of events updating the GTCNT register.

Table 23.77 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (writing to GTCNT/GTCLR)	High
Clear by hardware sources set in GTCSR	↑
Count up or down by hardware sources set in GTUPSR/GTDNSR	↑
Count operation	Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change. When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), the writing by CPU has priority over the starting/stopping by hardware sources.

In case that stop by the period count function conflicts with start by the CPU writing (GTCR register writing/GTSTR register writing), the period count function is finished with setting the GTST.PCF flag. The CST bit is not changed and the GTCNT continues to count.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. When there is a conflict between updating the GTCR.CST bit and reading by the CPU (reading from GTCR/GTSTR/GTSTP registers), pre-update data is read.

(3) GTCCRm registers (m = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to the GTCCRm registers, the writing to GTCCRm registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. When there is a conflict between updating the GTCCRm registers and reading by the CPU, pre-update data is read.

(4) GTPR register

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

(5) GTADTRm registers (m = A, B)

When there is a conflict between buffer transfer operation and writing to GTADTRm register, writing to GTADTRm register has priority over buffer transfer operation.

When there is a conflict between updating the GTADTRm register and reading by the CPU, pre-update data is read.

(6) GTDVm registers (m = U, D)

When there is a conflict between buffer transfer operation and writing to GTDVm register, writing to GTDVm register has priority over buffer transfer operation.

When there is a conflict between updating the GTDVm register and reading by the CPU, pre-update data is read.

(7) GTIOR.GTIOm registers (m = A, B)

When there is a conflict between buffer transfer operation and writing to GTIOR.GTIOm register, writing to GTIOR.GTIOm register has priority over buffer transfer operation.

When there is a conflict between updating the GTIOR.GTIOm and reading by the CPU, pre-update data is read.

23.10.6 Interval of Interrupt Request

When the core clock of GPT is GPTCLK, interrupt may be lost if the interval between the same interrupt signal is shorter than the following value. However, this restriction does not apply to different interrupt signals.

Interrupt_Interval [ns] = Period_of_GPTCLK [ns] * 6 + Period_of_PCLKA [ns] * 4

Also, ADC can receive the A/D conversion start request from GPT without going through ELC by setting ADTRGGPTx register (x = 0 to 8).

Again, when the clocks of GPT and ADC are combined as shown in Table 23.78, the A/D conversion start request may be lost if the interval between one A/D conversion start request and the next is less than the following value for the same A/D conversion start request.

However, this restriction does not apply to different A/D conversion start request.

Event_Interval [ns] = Period_of_GPT_core_clock [ns] * 6 + Period_of_ADC_core_clock [ns] * 4

Table 23.78 Combination of clocks with the restricted Event Interval

GPT core clock	ADC core clock
GPTCLK	PCLKA or ADCCLK
PCLKD	ADCCLK or GPTCLK

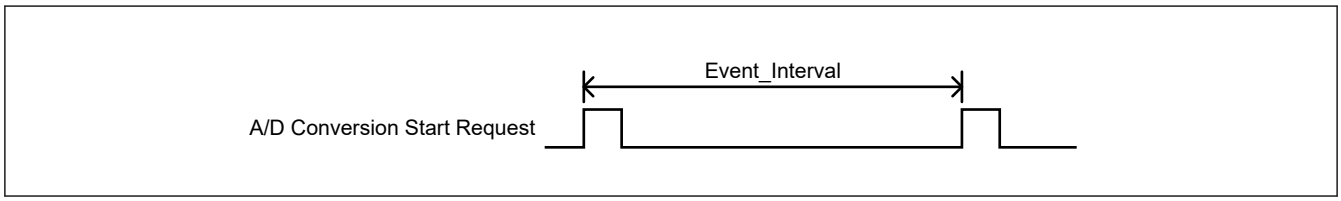


Figure 23.172 Example of A/D Conversion Start Request Event Interval

23.10.7 Notes on the GTIOCnm Signal Input to PWM Delay Generation Circuit (n = 0 to 3, m = A, B)

When controlling the delay of PWM waveform in PWM Delay Generation Circuit, the following limitations exist.

- In saw-wave mode, It is prohibited to change the GTIOCnm signal during the three clock cycles immediately before overflow or underflow.
- In saw-wave mode, it is prohibited to clear the GTCNT register by GTCSR during counting operation.
- In triangle-wave mode, It is prohibited to change the GTIOCnm signal during the three clock cycles immediately before trough.

If the above limitations are not followed, the edge of signal waveform output from PWM Delay Generation Circuit may disappear.

Figure 23.173 shows an example of the change timing of an unacceptable GTIOCnm signal.

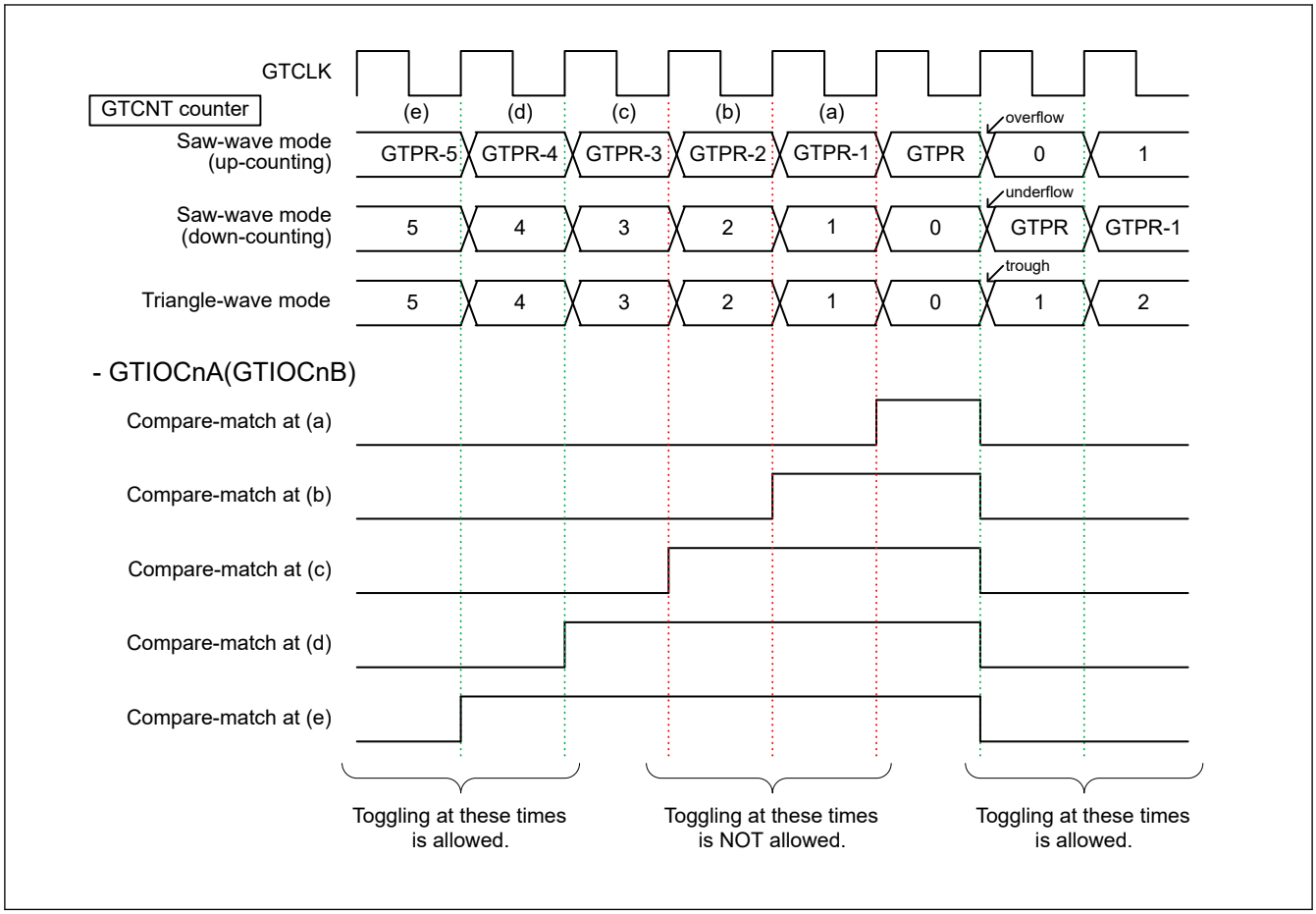


Figure 23.173 Example of unacceptable GTIOCnm signal timing (n = 0 to 3, m = A, B)

23.10.8 Setting Range of the Compare Match Registers when GTIOR.CPSCIR=1

In complementary PWM mode, when GTIOR.CPSCIR=1 and the initial output of the GTIOCnA/GTIOCnB pins after synchronization clearing is disabled, set the compare match registers (GTCCRA, GTCCRC, GTCCRD, GTCCRE, GTCCRF) to at least twice the GTDVU value.

23.10.9 Strobe Signal for Testing to PWM Delay Generation Circuit

Each channel output PWM output, PWM cycle synchronous signal (the cycle end), PWM output strobe signal for testing, register write protection signal (GTWP.WP bit) to the PWM Delay Generation circuit (PDG).

The strobe signals monitor each rising edge or falling edge of GTIOCxA output and GTIOCxB output. One GTCLK later from changing of PWM output, the strobe signal becomes 1. At the count clock of the cycle end, it becomes 0. The conditions that the strobe signal becomes 0 are reset and the cycle end.

When GTCNT counting is stopped, the status of strobe signal is retained. When GTCNT counting is restarted and PWM output is generated after GTCNT is stopped under the condition that strobe signal is 1, during first period after restarting to count, strobe signal does not change from 1. So the edge of PWM output is not monitored correctly. At the first cycle end after restarting, strobe signal returns to 0. The strobe signal is generated correctly from the second cycle.

In order to reset strobe signal keeping the status of 1 during GTCNT stopping, generate the cycle end by GTCNT counting as shown in Figure 23.174 or clear counter for sawtooth-wave operation as shown in Figure 23.175.

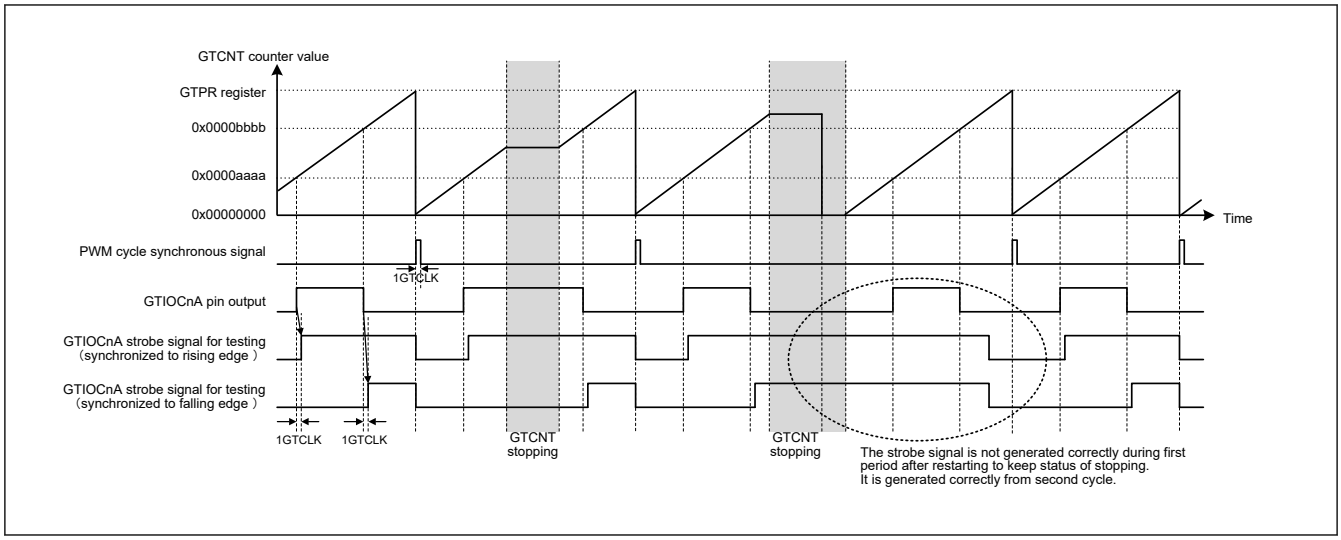


Figure 23.174 Example of output operation to PDG (1)

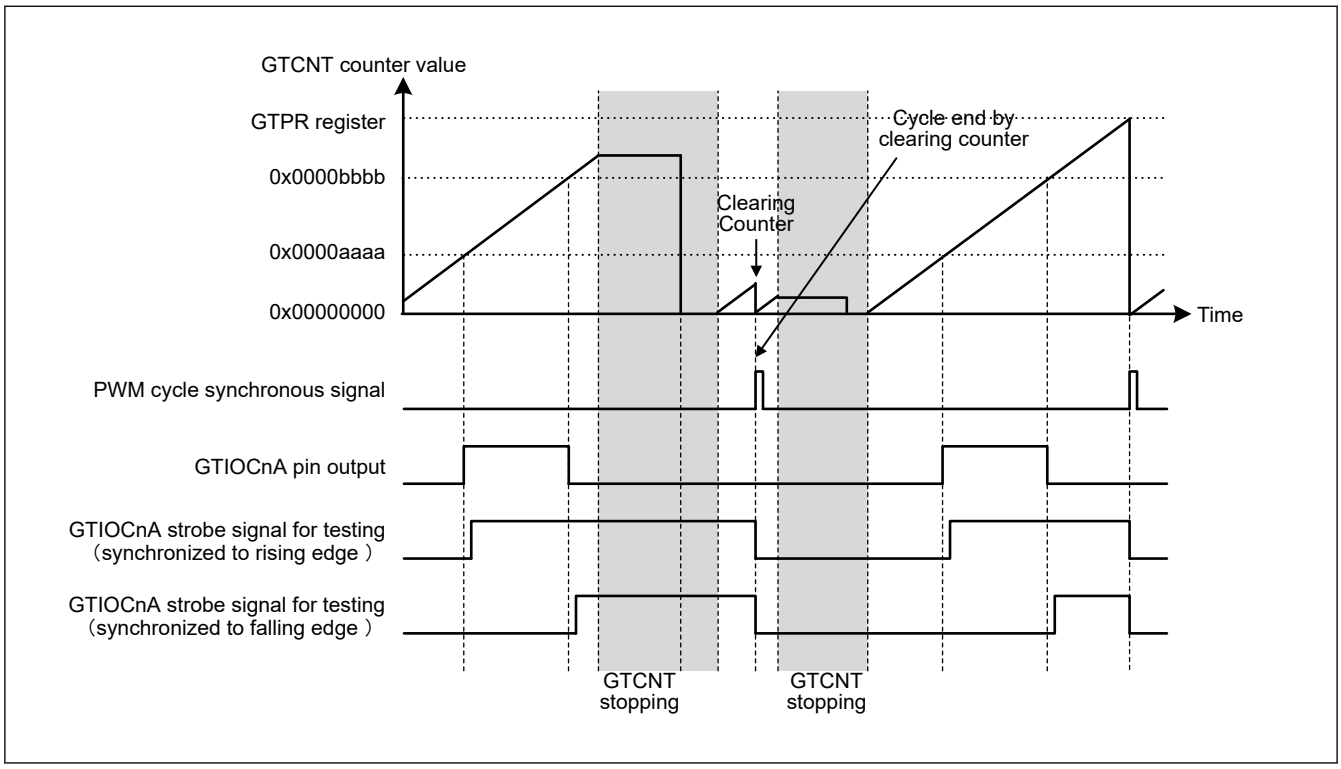


Figure 23.175 Example of output operation to PDG (2)

23.10.10 Notes on Transitioning to Standby Mode

Before transitioning to standby mode, it should be stopped counter operation (Set GTCR.CST = 0).